

MODEL NAME : ZIJI1
PCB NO : LA-A661P
BOM P/N : xxx



Compal Confidential

ZIJI1 Schematics Document

Intel Bay Trail

2013-05-09

REV: A

@ : Nopop Component
3G@ : Pop on 3G model

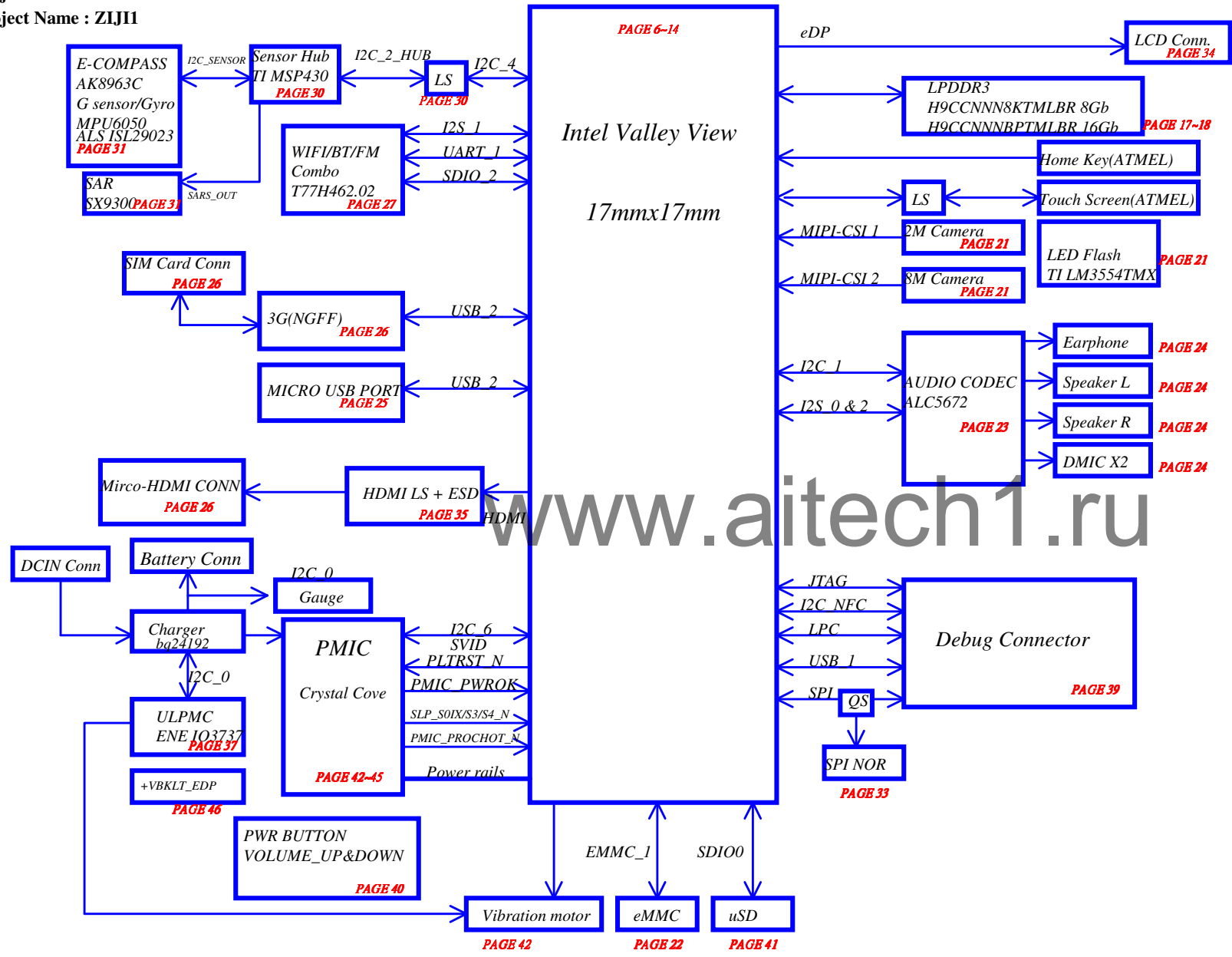
Revision history

Version	Date	Description
A	2013/03/27	* Initial release
B		

Model Name :
Project Code:
Project Name : ZIJ11

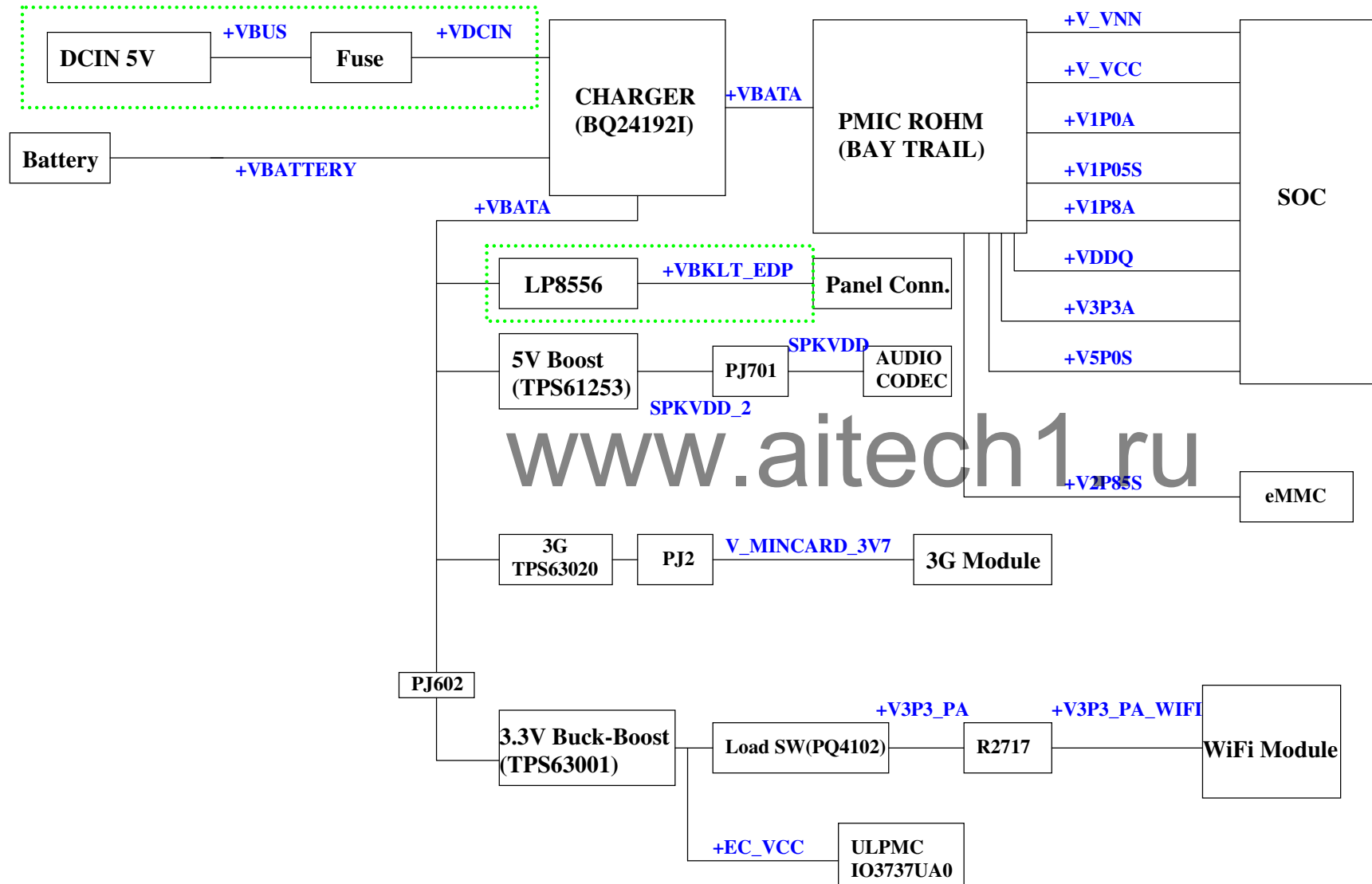
ZIJ11 Bay Trail-T Block Diagram

LS-----Level Shifter



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ZIJ11 POWER TREE



Title		
ZIJ11 Power Tree		
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V0JV3 POWER SEQUENCE

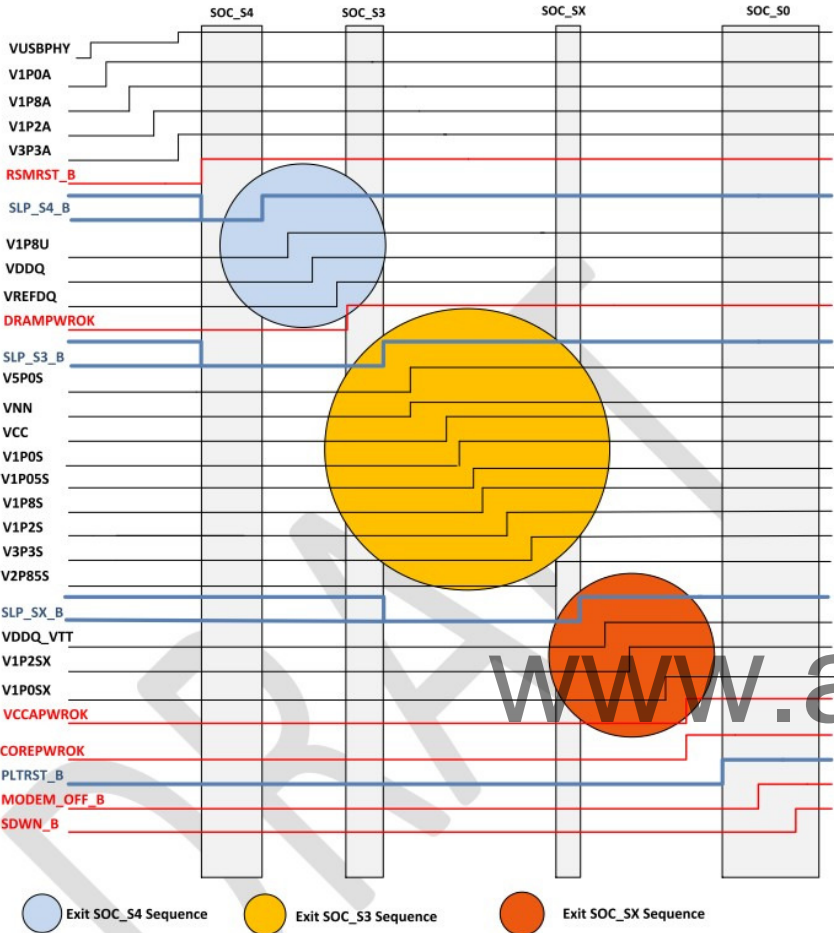
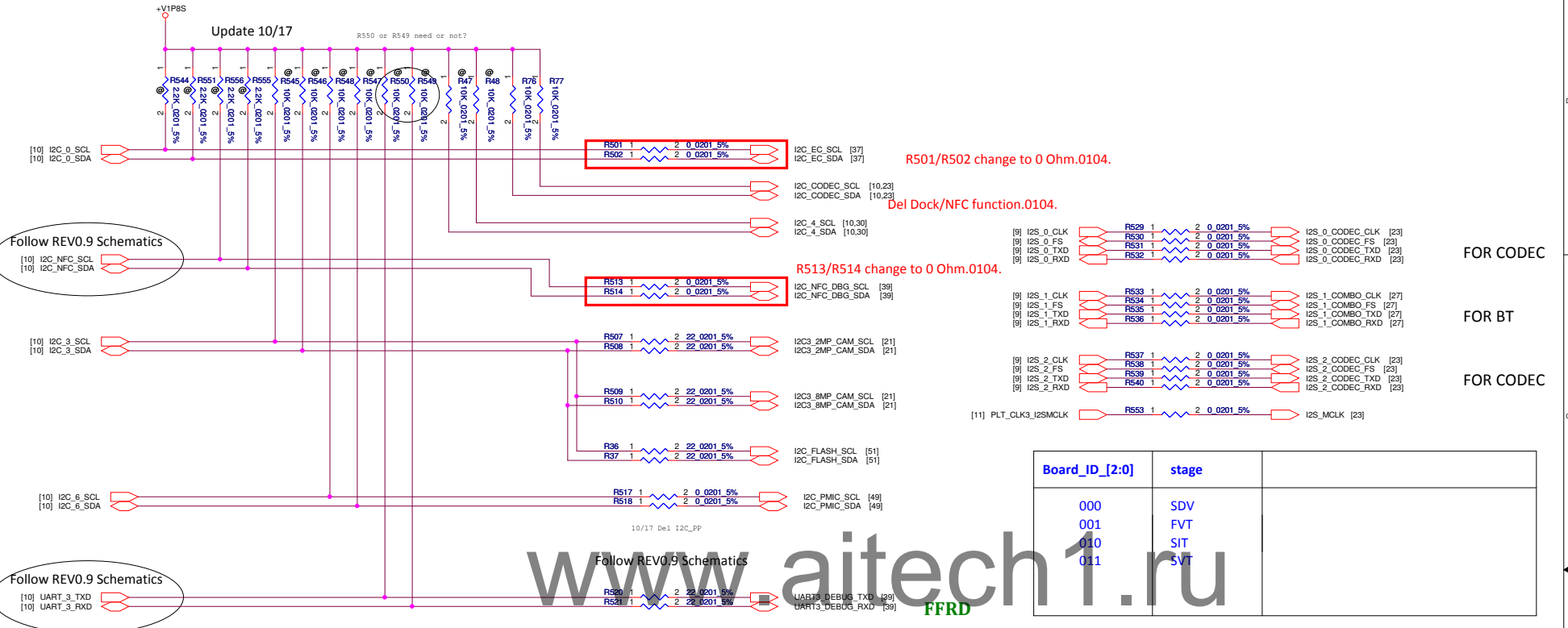


Figure 9: Cold Boot Power Sequencing Diagram

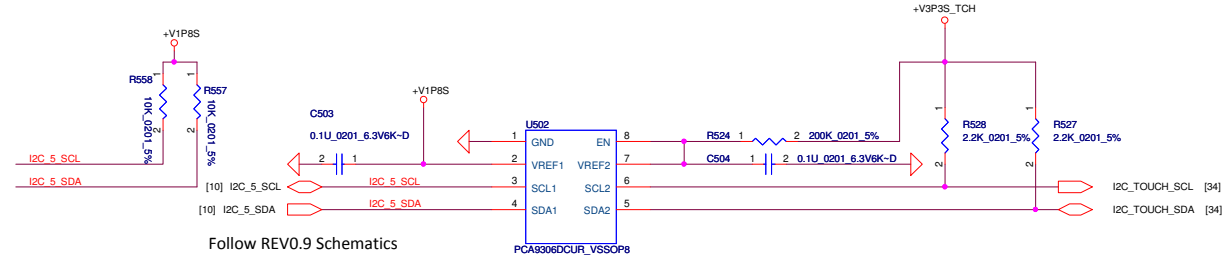
Voltage Rail ON/OFF On Various Power States

Num.	Voltage domain	Supply Module	PWR TYPE	S0	S0ix	S3	S4/5	G3
1	+VCC	VLV2	SVID BUCK	ON	OFF	OFF	OFF	OFF
2	+VNN	VLV2	SVID BUCK	ON	ON	OFF	OFF	OFF
3	+V1PoA	VLV2	BUCK	ON	ON	ON	ON	OFF
4	+V1Po5S	VLV2	BUCK	ON	ON	OFF	OFF	OFF
5	+V1P8A	VLV2	BUCK	ON	ON	ON	ON	OFF
6	+VDDQ	VLV2/DDR	BUCK	ON	ON	ON	OFF	OFF
7	+V3P3A	VLV2, Peripheral	BUCK-BOOST	ON	ON	ON	ON	OFF
8	+V2P85S	Peripheral	BUCK-BOOST	ON	ON	OFF	OFF	OFF
9	+V5PoS	Peripheral	BOOST	ON	ON	OFF	OFF	OFF
10	+VSDIO	Peripheral	FET SW	ON/OFF	ON/OFF	OFF	OFF	OFF
11	+VDDQ_VTT	DDR3	LDO	ON	OFF	OFF	OFF	OFF
12	+V1P2A	VLV2	LDO	ON	ON	ON	ON	
13	+VREF		LDO					
14	+VUSBPHY	Peripheral	FET SW	ON	ON	ON	ON	ON
15	+VSYS_U	Peripheral	EXT FET SW	ON/OFF	ON/OFF	ON	OFF	OFF
16	+VSYS_S		FET SW	ON/OFF	ON/OFF	OFF	OFF	OFF
17	+V1P2S		FET SW	ON	ON	OFF	OFF	OFF
18	+V1P2SX		FET SW	ON	OFF	OFF	OFF	OFF
19	+V1P8S	VLV2	FET SW	ON	ON	OFF	OFF	OFF
20	+V1P8SX		FET SW	ON/OFF	ON/OFF	OFF	OFF	OFF
21	+V2P85SX	Peripheral	FET SW	ON/OFF	ON/OFF	OFF	OFF	OFF
22	+V3P3U	Peripheral	EXT FET	ON/OFF	ON/OFF	ON	OFF	OFF
23	+VHDMI	Peripheral	FET SW	ON/OFF	ON/OFF	OFF	OFF	OFF
24	+V1P8U	Peripheral	EXT FET SW	ON	ON	ON	OFF	OFF
25	+V1PoS	VLV2	EXT FET SW	ON	ON	OFF	OFF	OFF
26	+V1PoSX	VLV2	EXT FET SW	ON	OFF	OFF	OFF	OFF
27	+V3P3S	VLV2	EXT FET SW	ON	ON	OFF	OFF	OFF
28	+VBUS	Peripheral	EXT SW	ON/OFF	ON/OFF	OFF	OFF	OFF
29	+VSYS_SX	Peripheral	EXT FET SW	ON/OFF	ON/OFF	OFF	OFF	OFF
30	+VREFDQ0		LDO	ON	ON	OFF	OFF	OFF
31	+VREFDQ1		LDO	ON	ON	ON	OFF	OFF

I2C & I2S MAP



PMIC_MEMCFG1(GPIO1P5)	PMIC_MEMCFG0(GPIO1P4)	Rank	Size
0	0	1	2G
0	1	2	4G



SOC:MEMORY

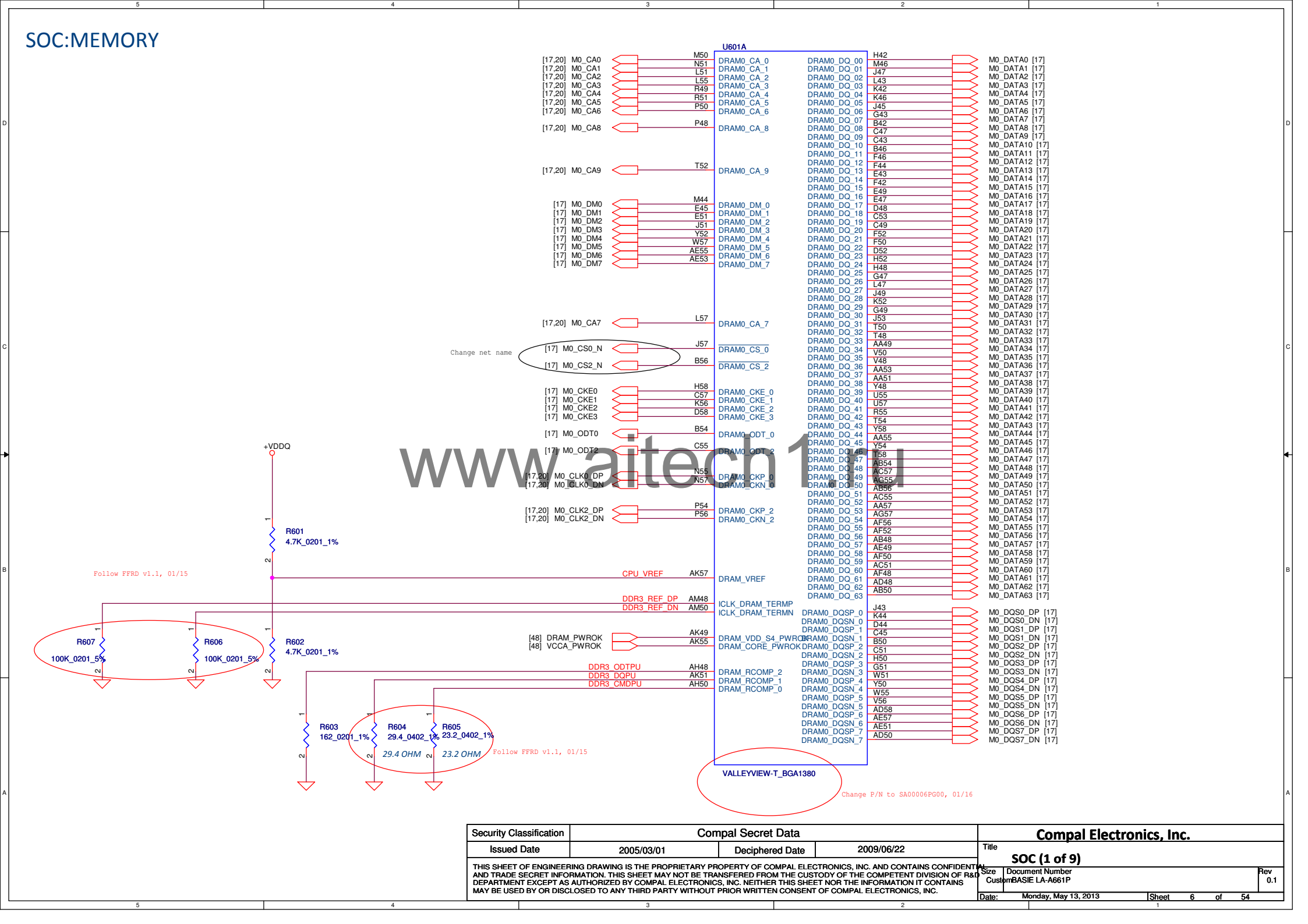
U601A

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SOC:MEMORY

U601A

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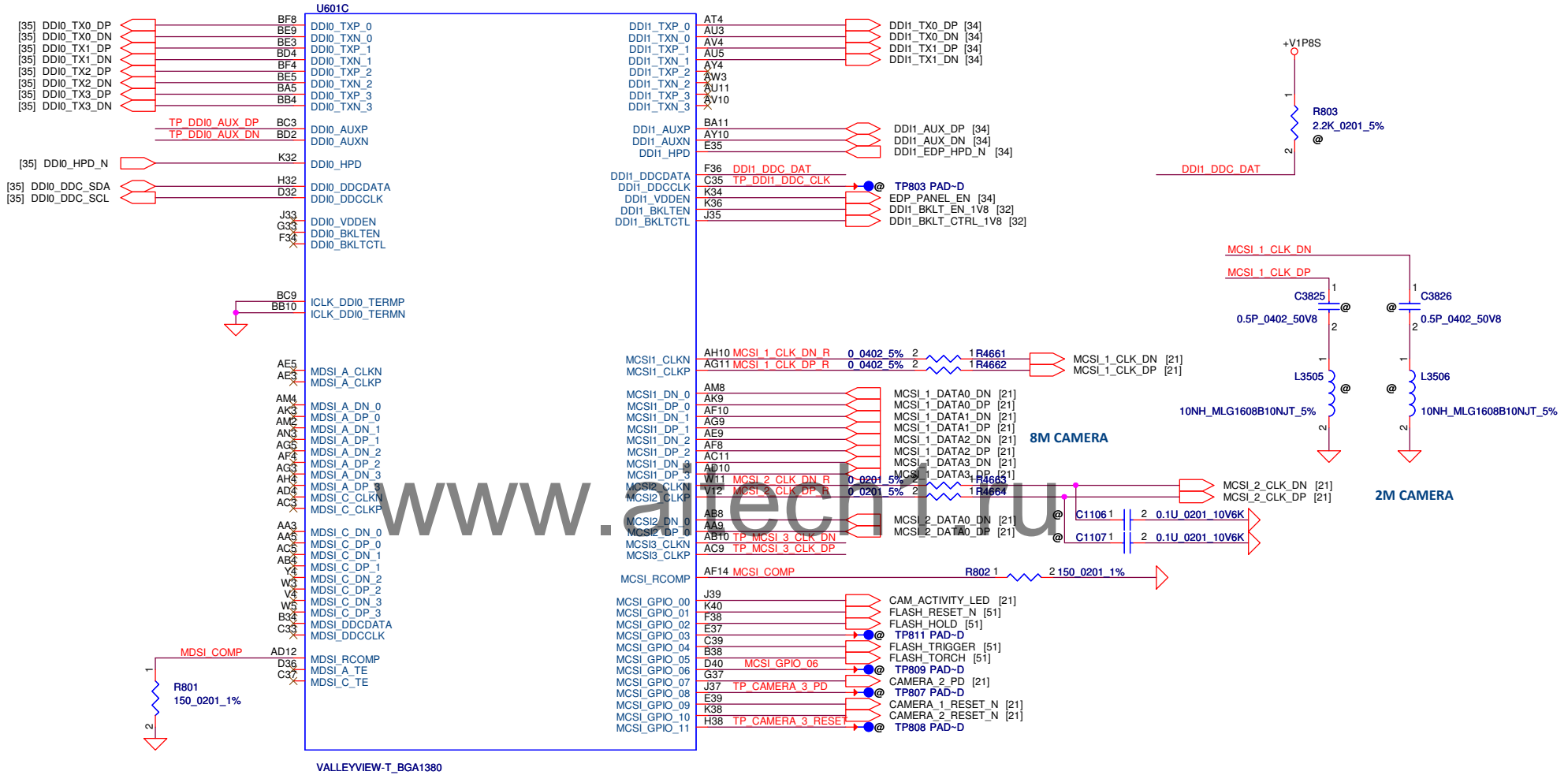
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1

SOC: DISPLAY AND CAMERA

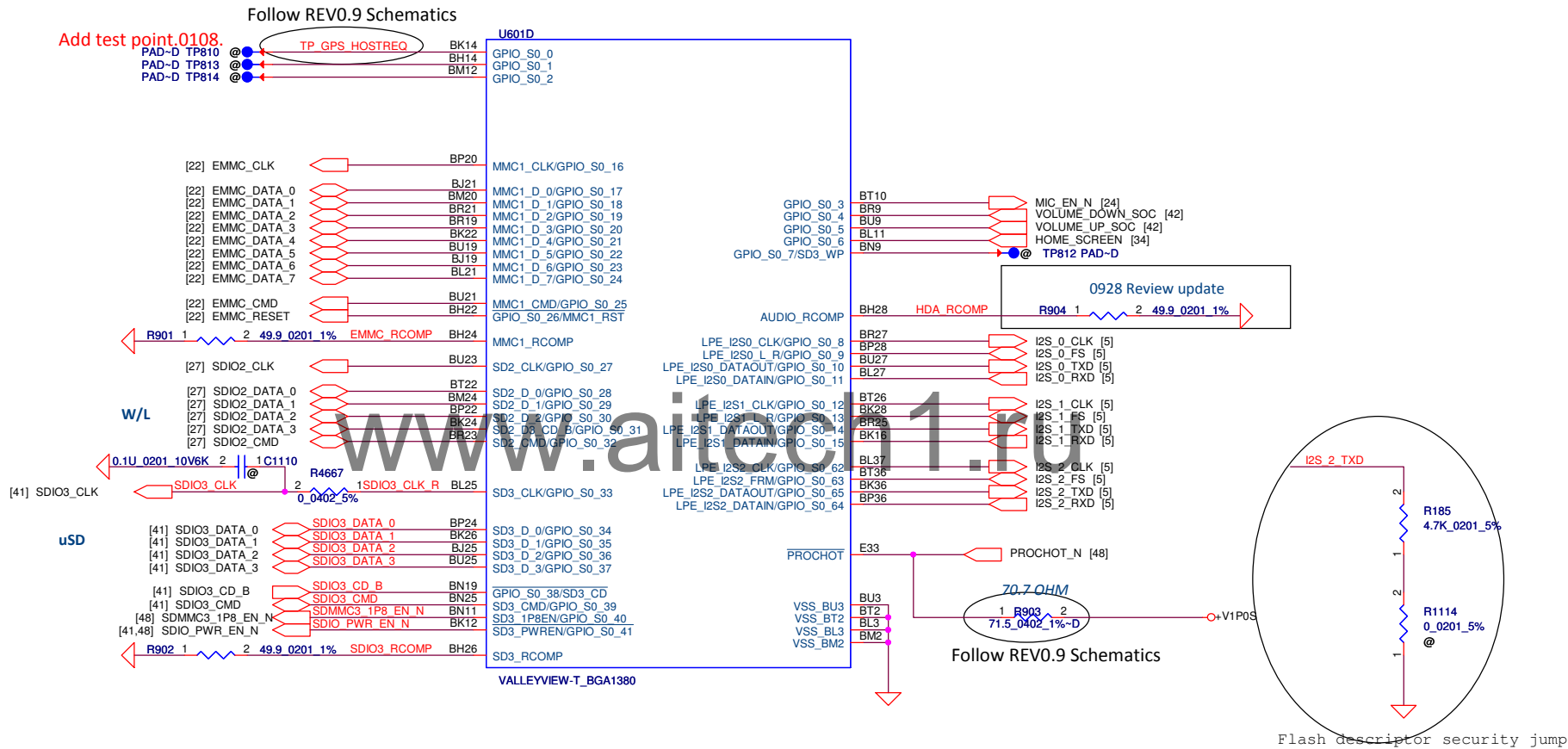
HDMI



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SOC:STORAGE AND AUDIO



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SOC:USB & I2C



Connector to LID_SW# and USB POGO.0111

Follow FFRD v1.1, 01/15

SIO_I2C6_DATA/GPIO_S0_90/NDM
 SIO_I2C6_CLK/GPIO_S0_91/SD3_WP
 NFD_I2C0_DATA/GPIO_S0_94
 NFD_I2C0_CLK/GPIO_S0_95

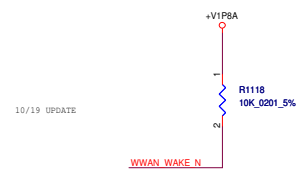
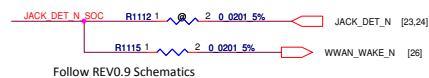
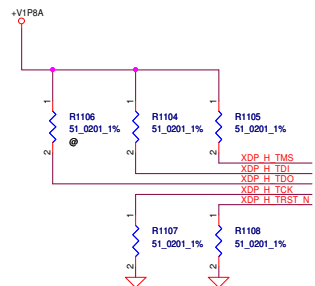
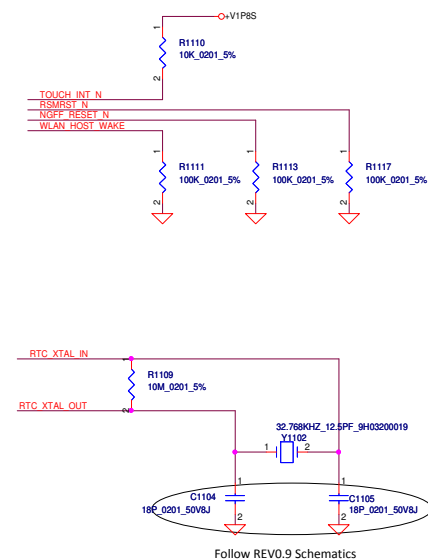
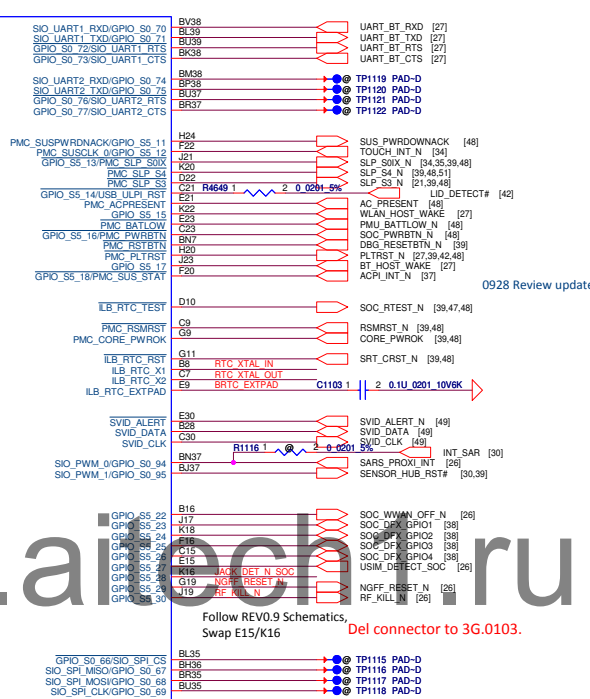
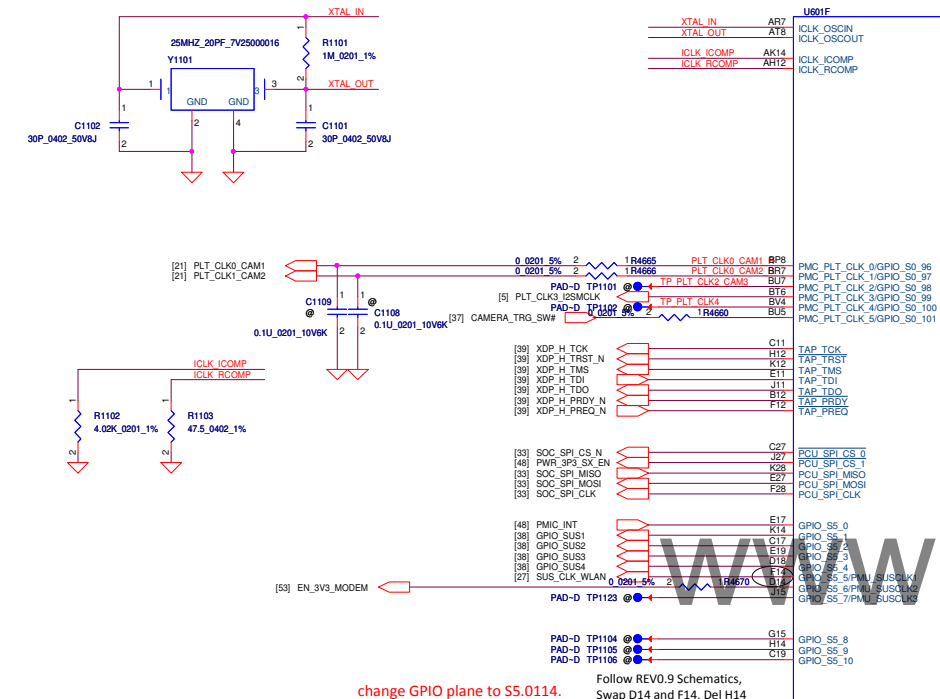
BR33
 BK34
 BK40
 BR39

I2C0_6_SDA [5]
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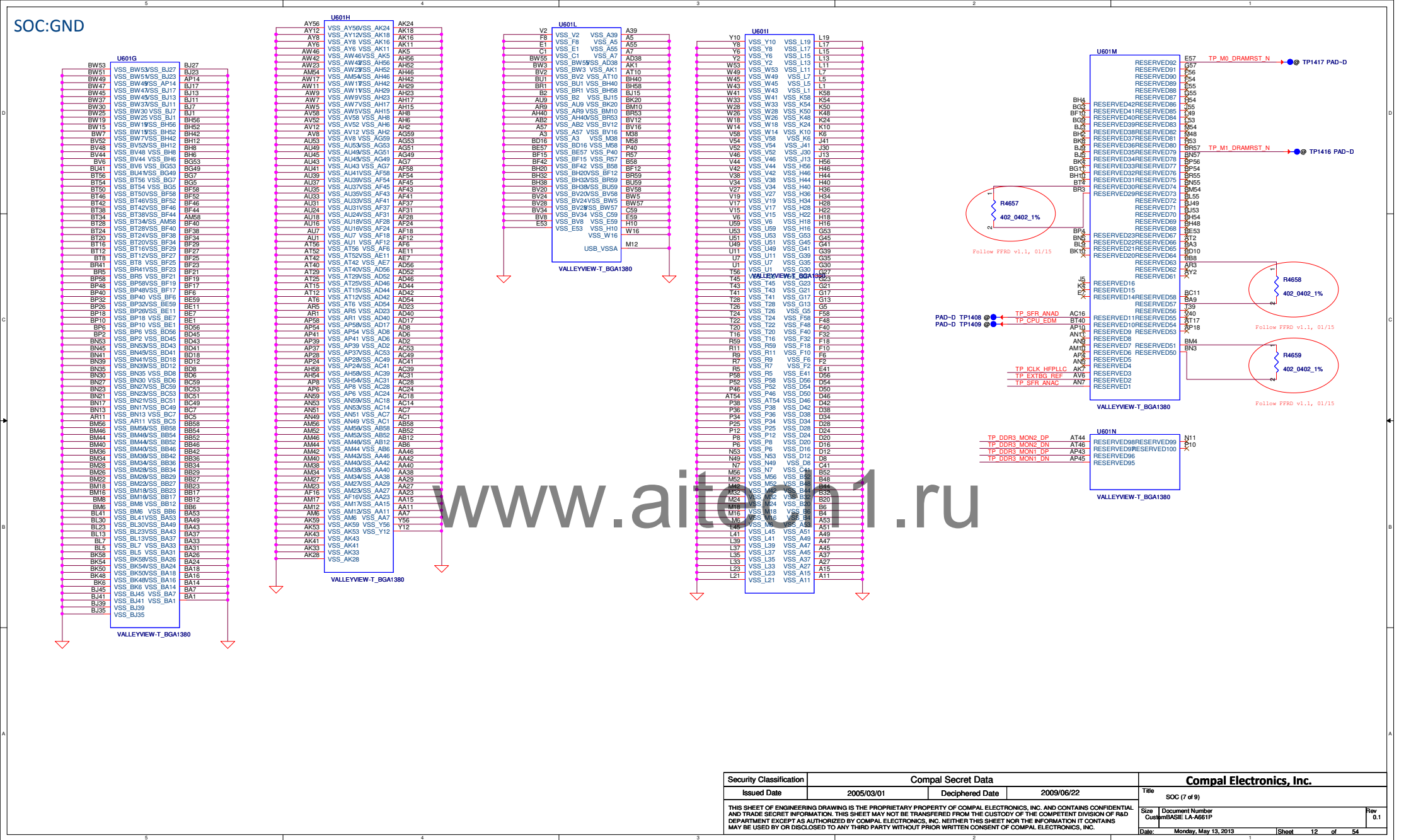
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SOC:CLOCK,DEBUG & MISC

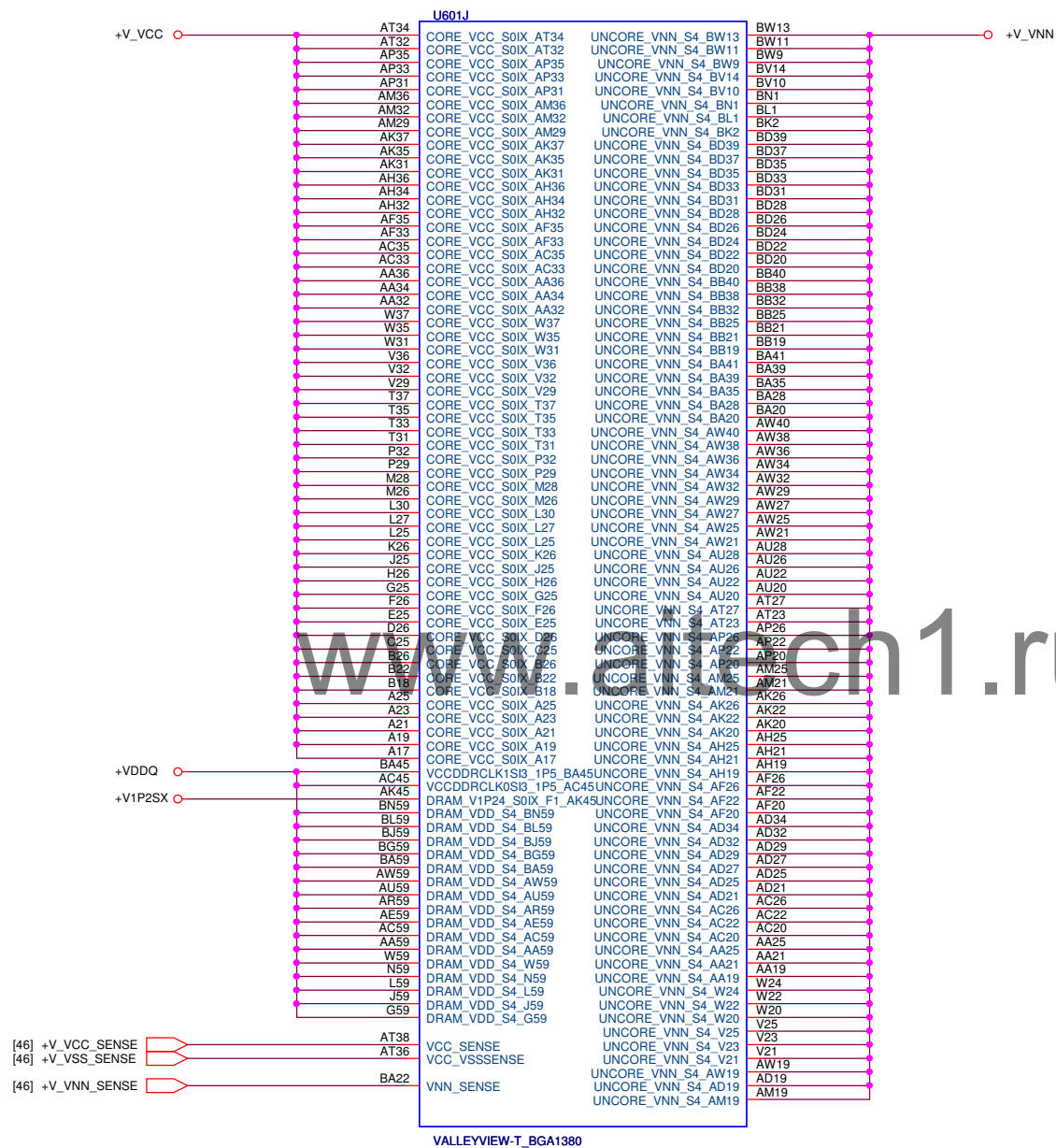


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SOC:GND



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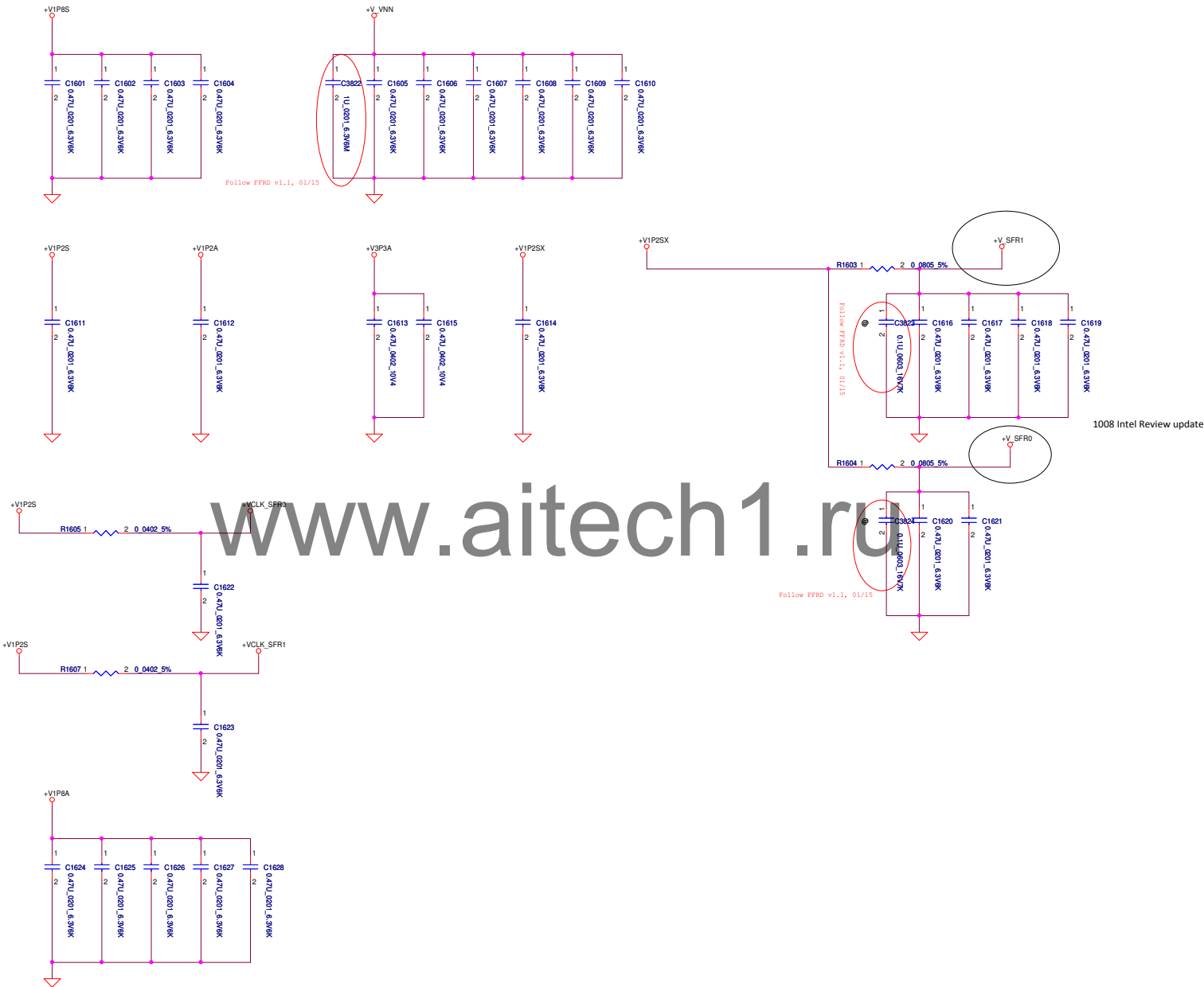
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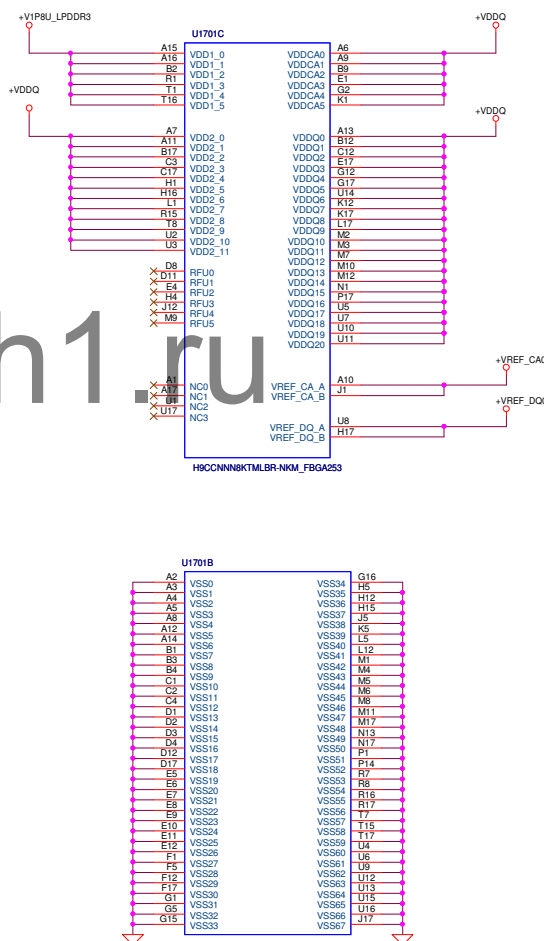
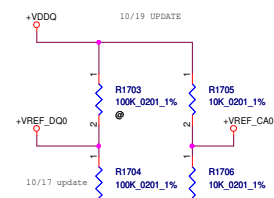
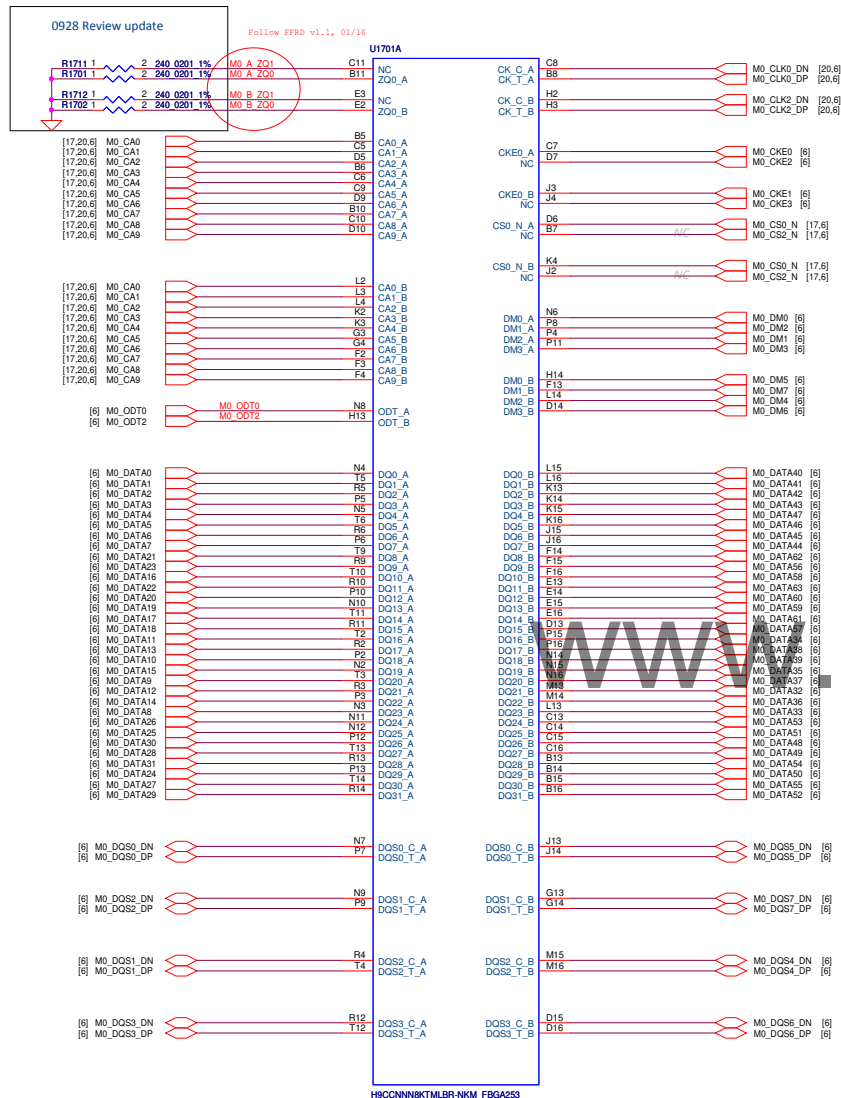


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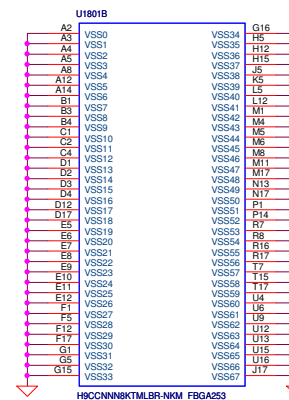
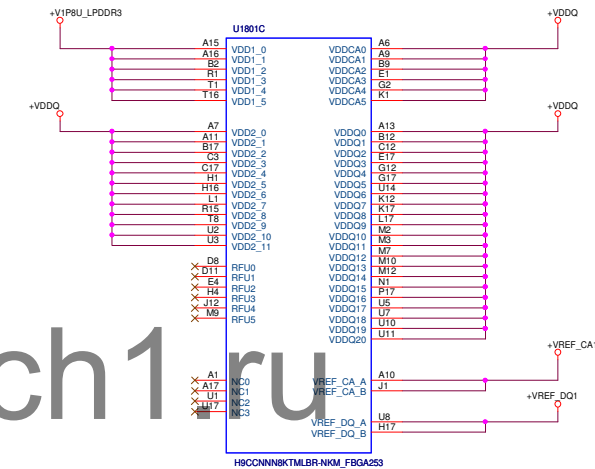
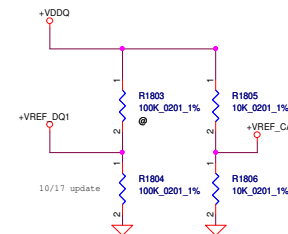
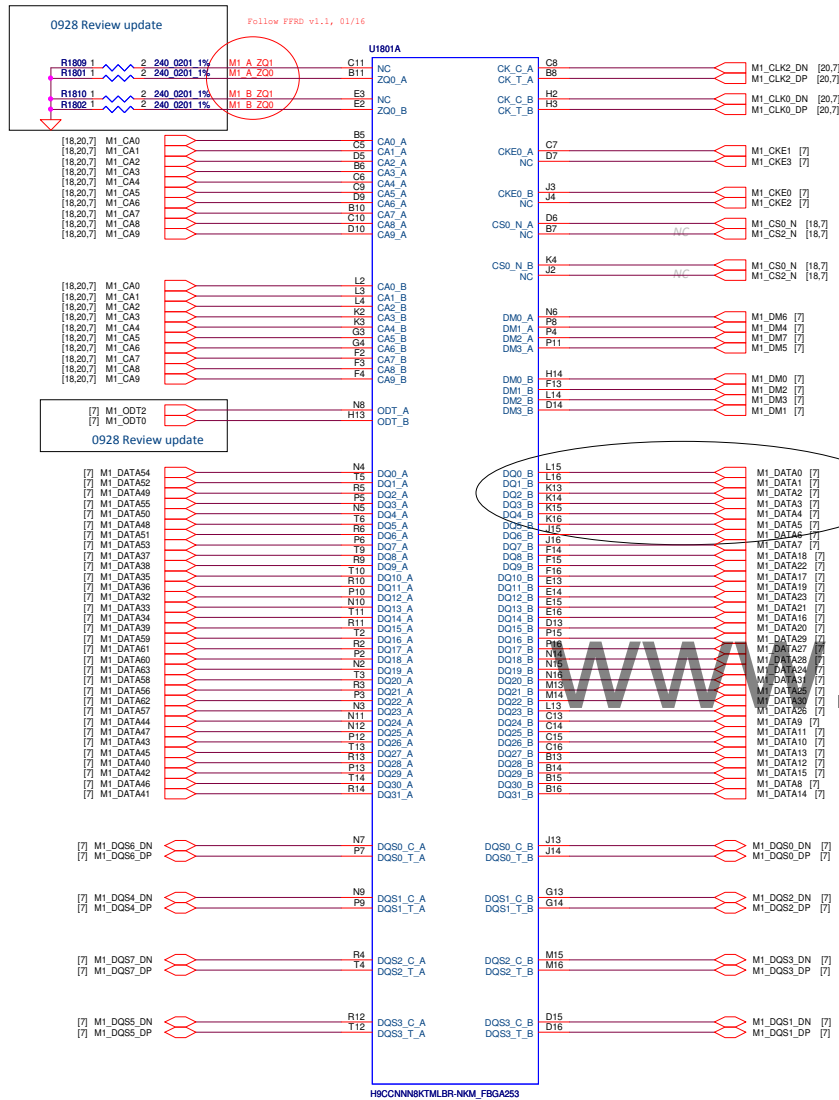
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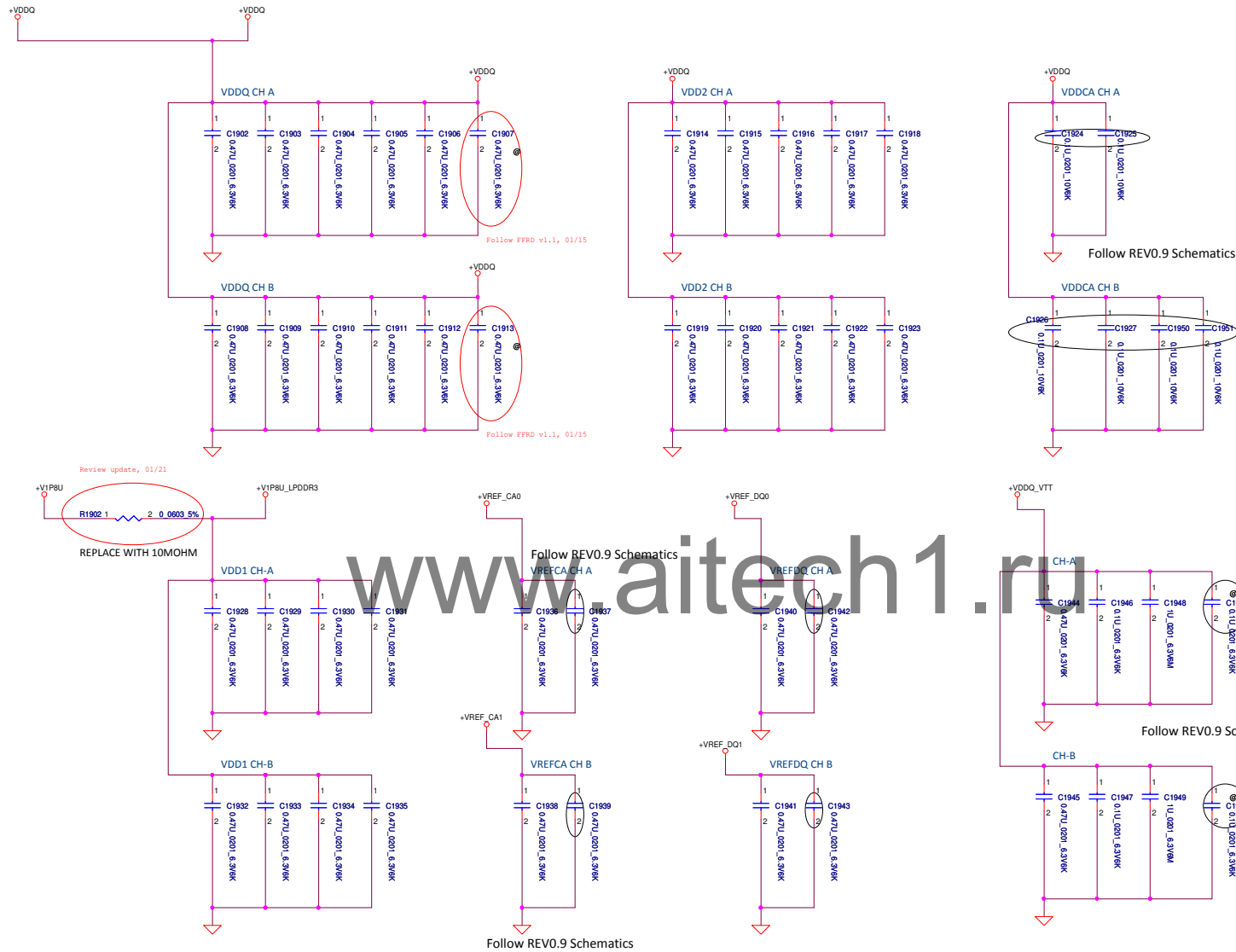




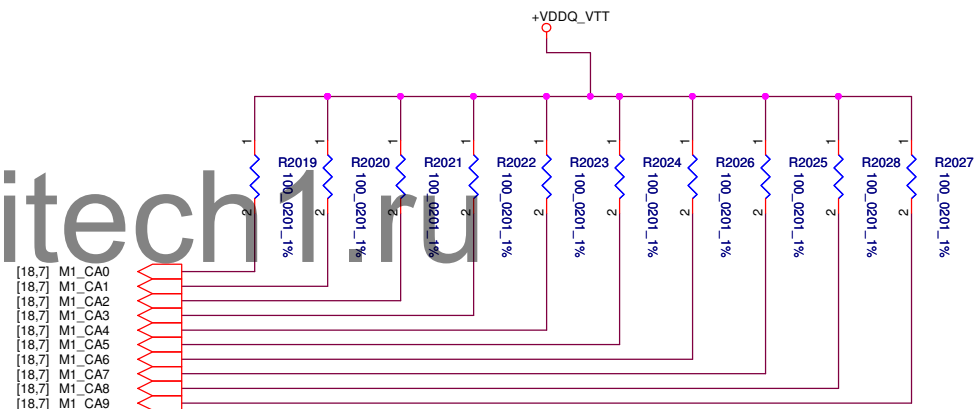
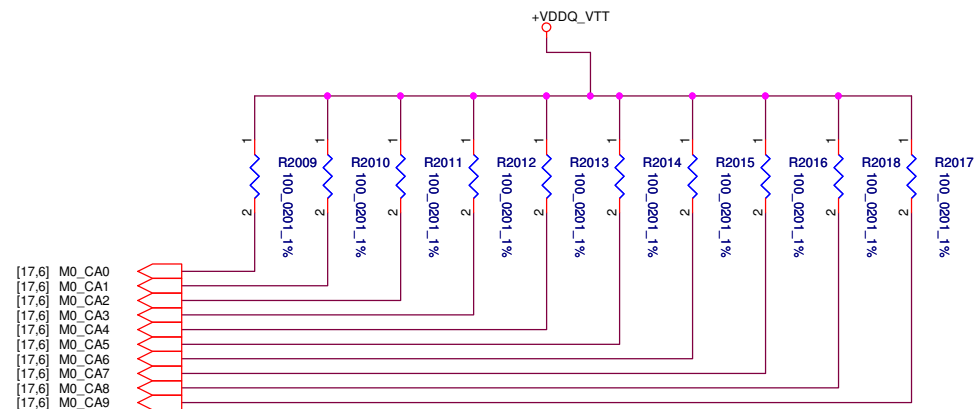
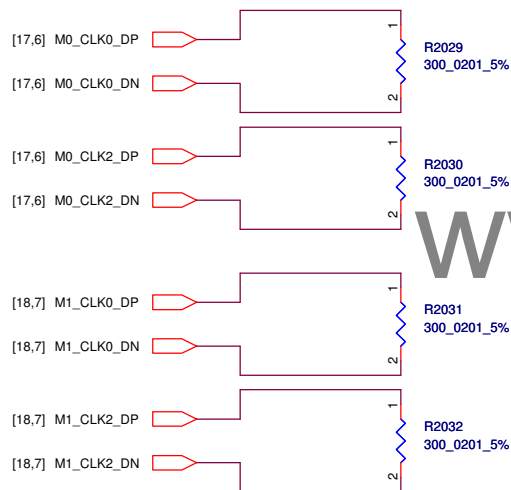
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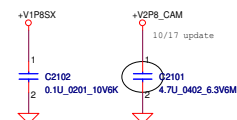




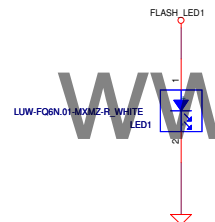
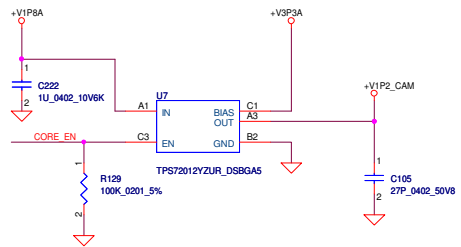
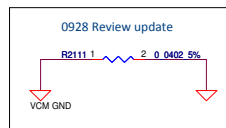
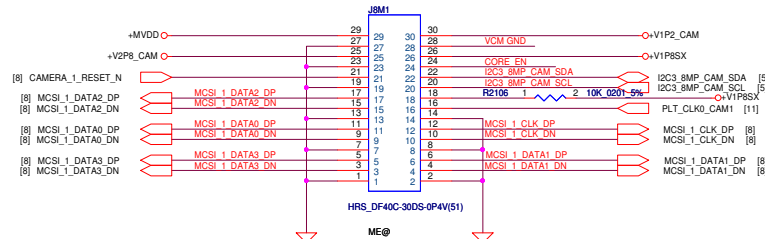
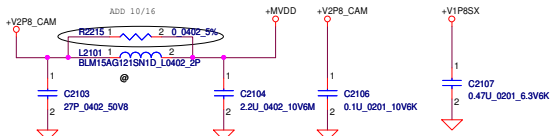
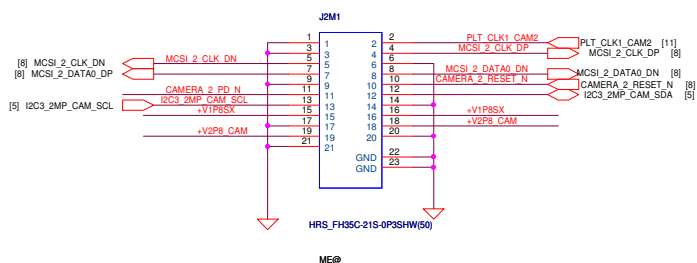
0928 Review update
Remove seris termination for CKE



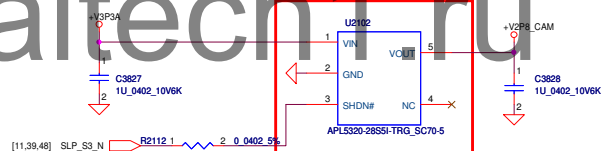
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2M CCM

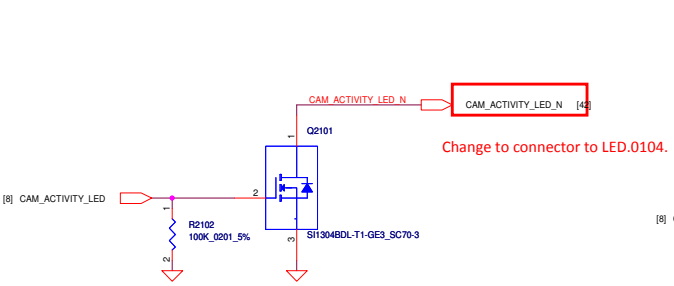


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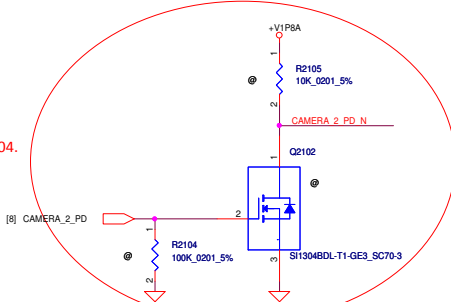


Chage active high parts.0111.

[Comapl component]



Change to connector to LED.0104.



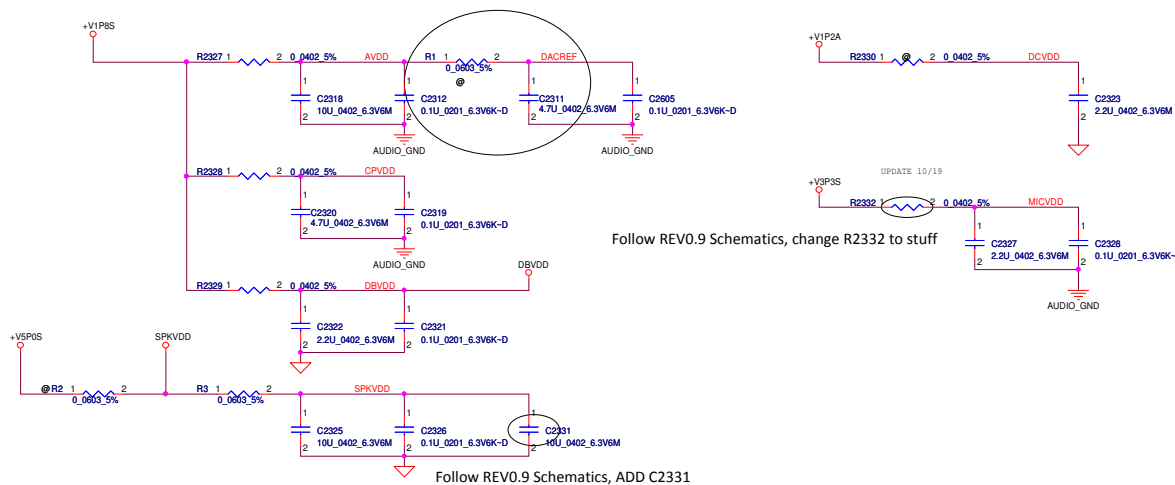
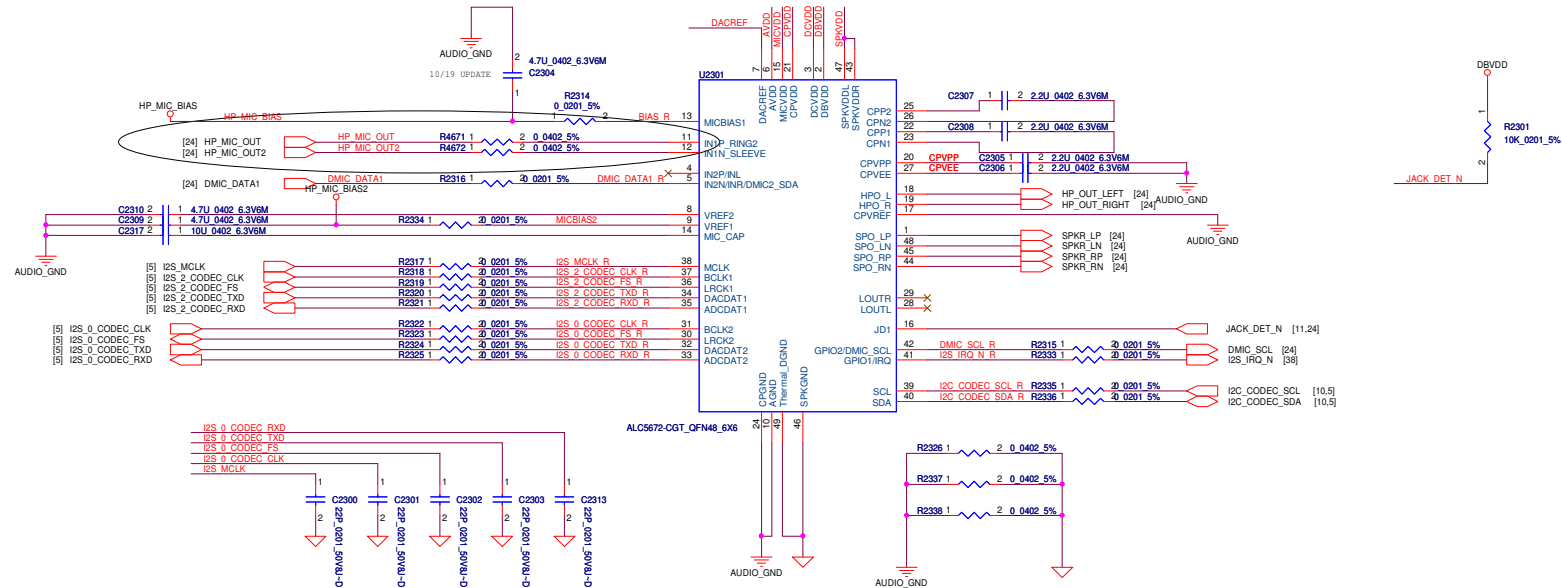
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Review update to mount, 0116

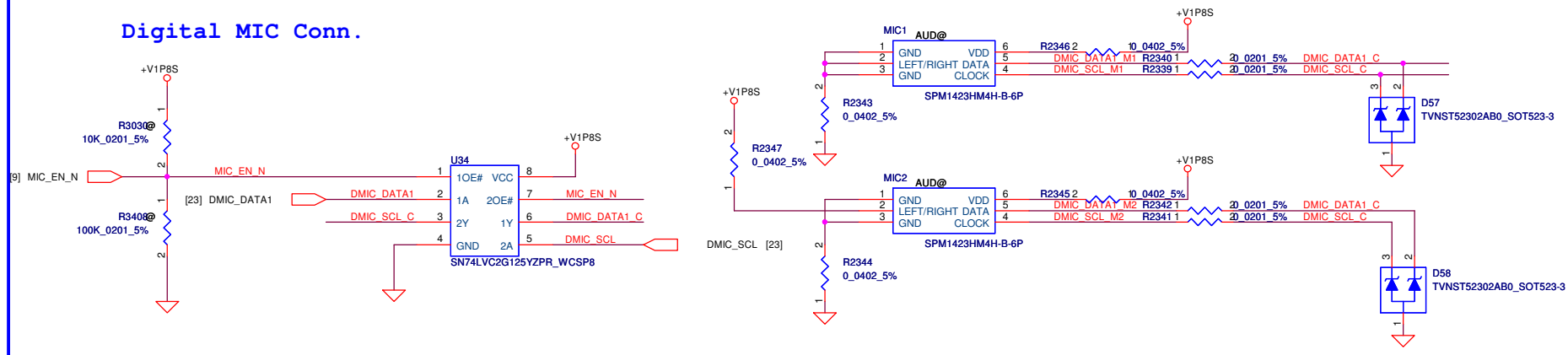
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Codec

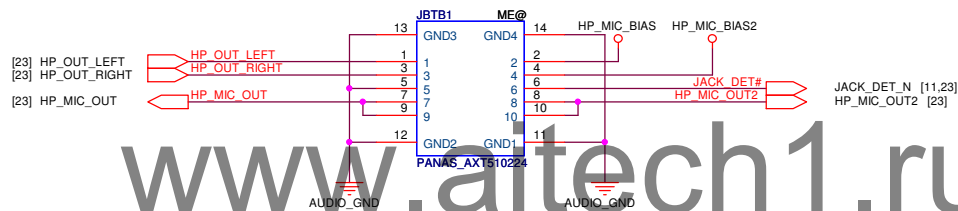


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				Date:	Monday, May 13, 2013

Digital MIC Conn.

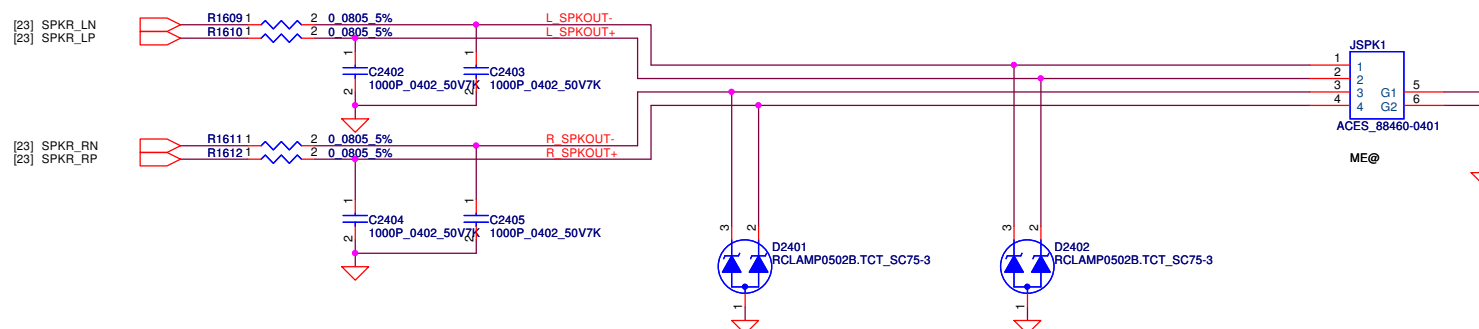


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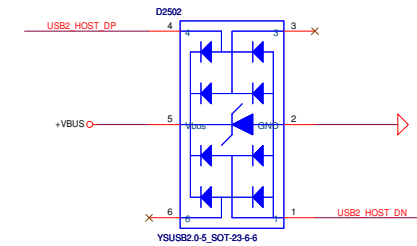
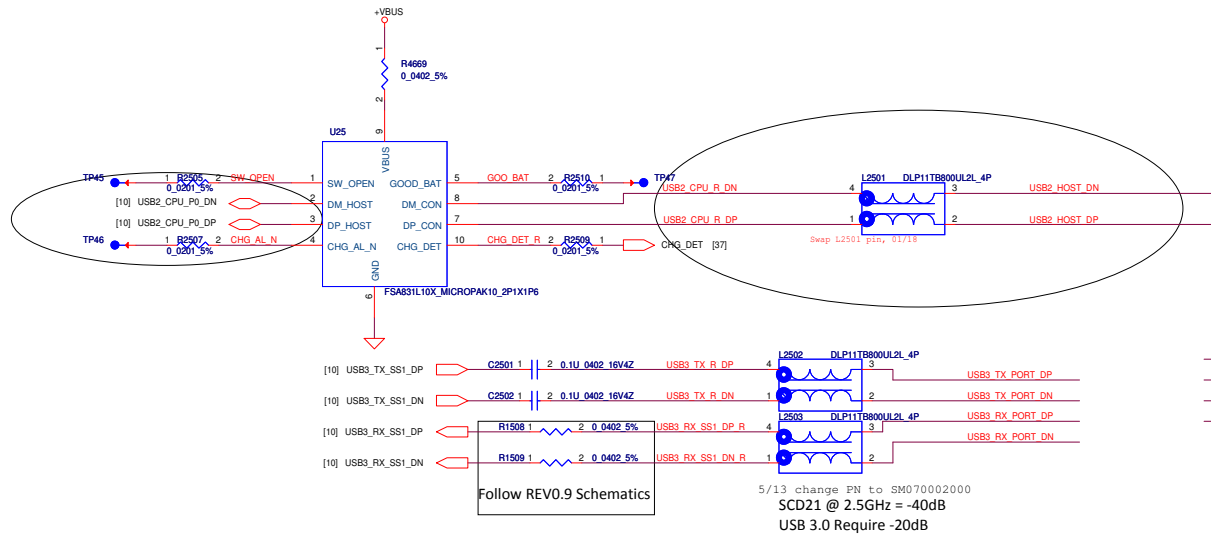


SPEAKERS

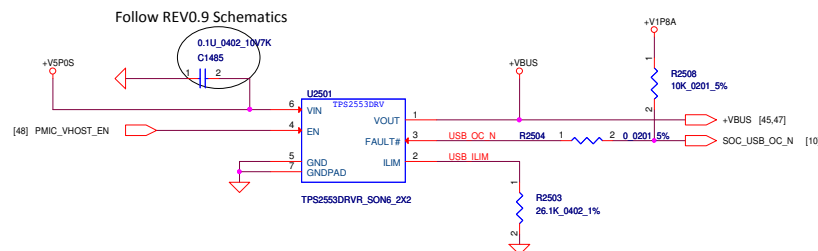
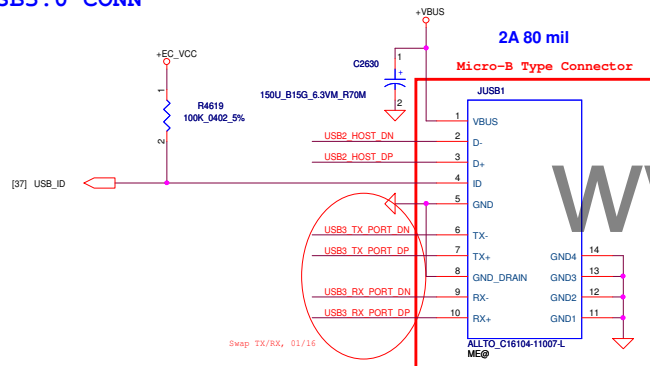
Follow REV0.9 Schematics
680P->1000P L->R



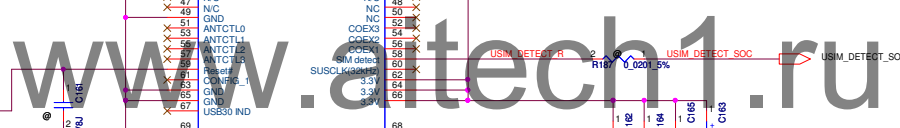
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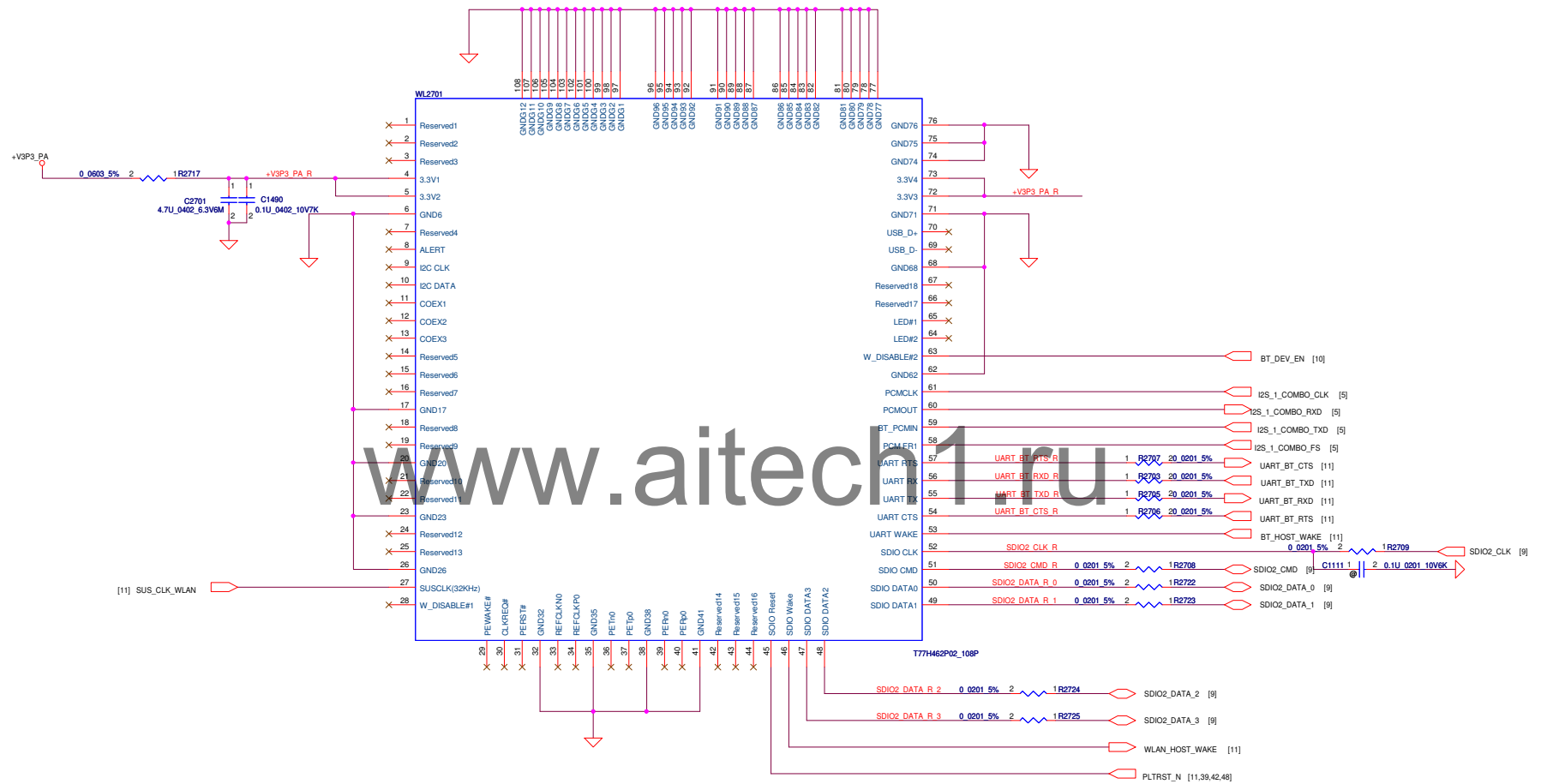
USB3.0 CONN

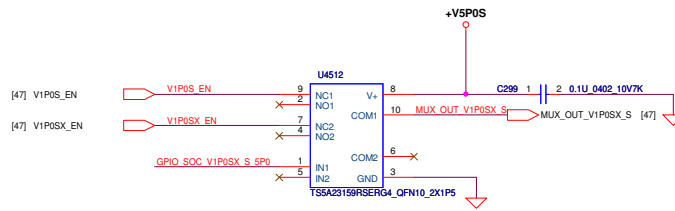
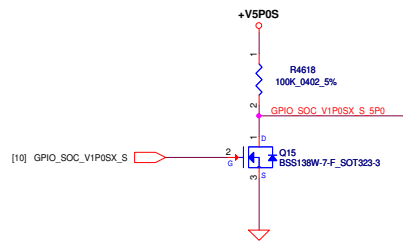


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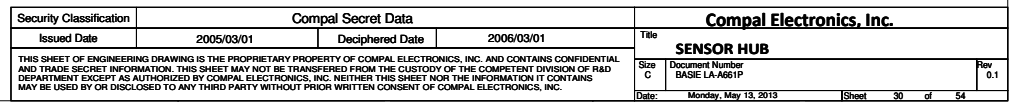
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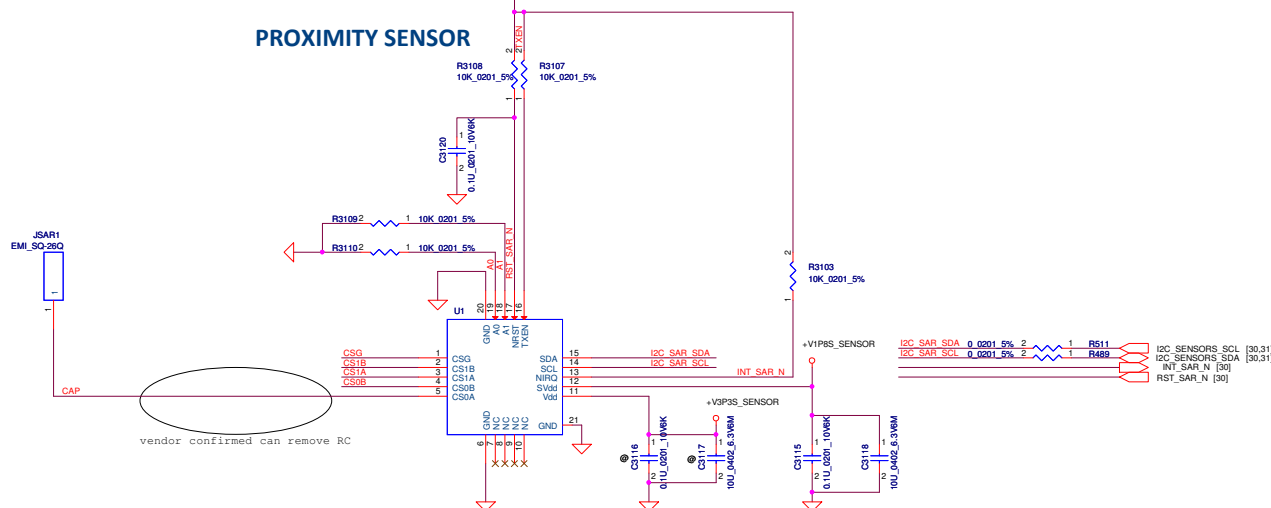
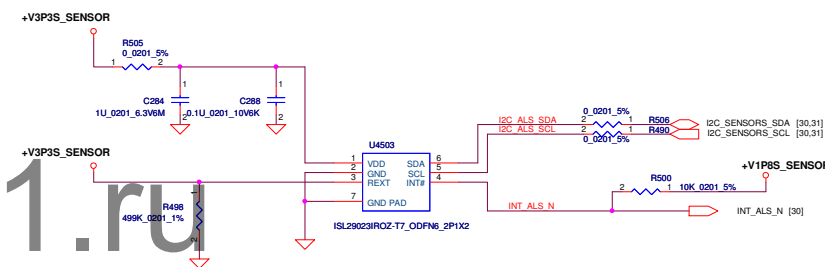
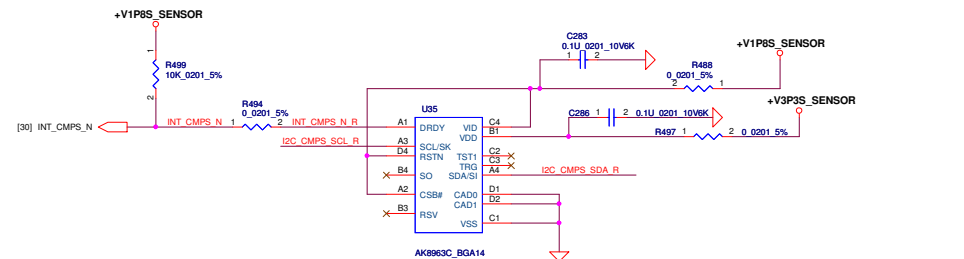
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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title	GPS
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NFC

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				C	BASIE LA-A661P	0.1
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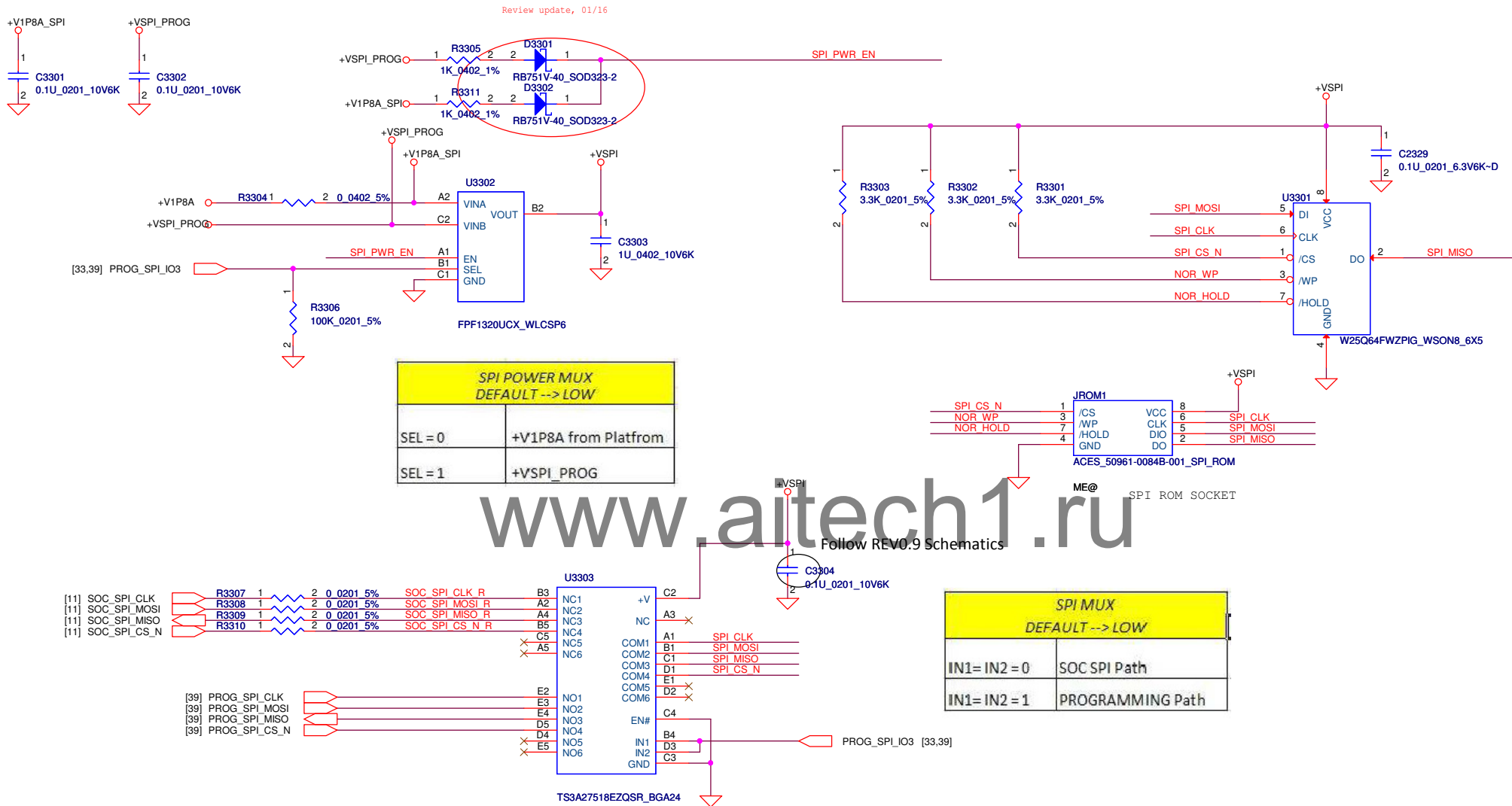




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DATE: MONDAY, MAY 13, 2013			SHEET 31 OF 54

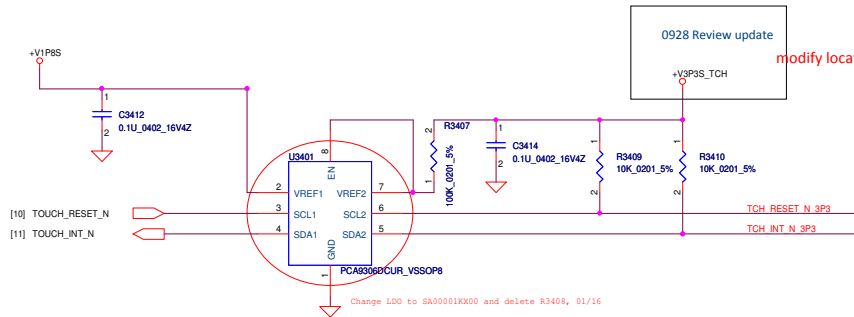
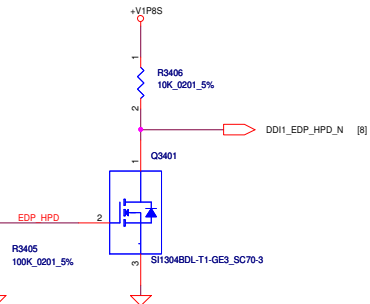
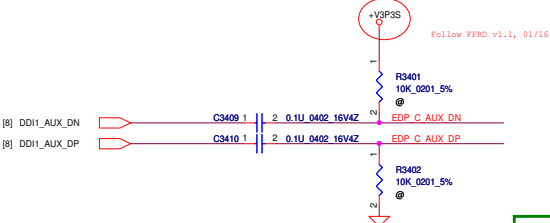
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				Date:	Monday, May 13, 2013	Sheet



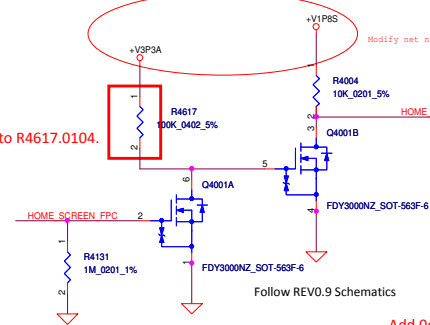
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[8] DDH1_TX1_DN C3405 1 2 0.1U 0402 16V4Z EDP C TX1 DN
 [8] DDH1_TX1_DP C3406 1 2 0.1U 0402 16V4Z EDP C TX1 DP
 [8] DDH1_TX0_DN C3407 1 2 0.1U 0402 16V4Z EDP C TX0 DN
 [8] DDH1_TX0_DP C3408 1 2 0.1U 0402 16V4Z EDP C TX0 DP



0928 Review update

modify location to R4617.0104.

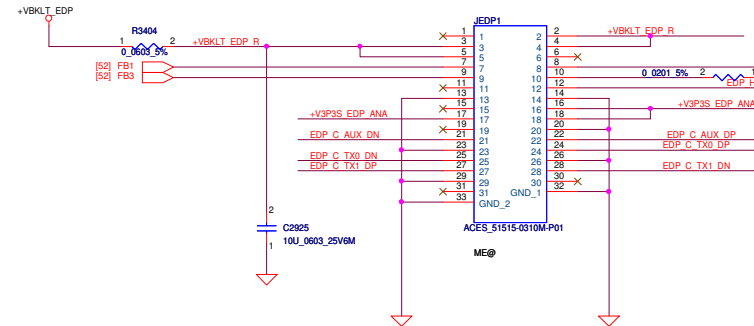


Follow REV0.9 Schematics

Add 0ohm to transfer +TP_PWR.0111.

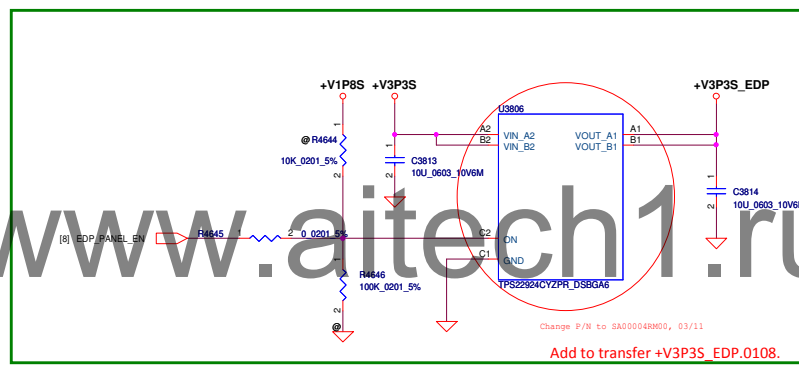
[42.48] HOME_SCREEN_FPC

Change net name .0102.

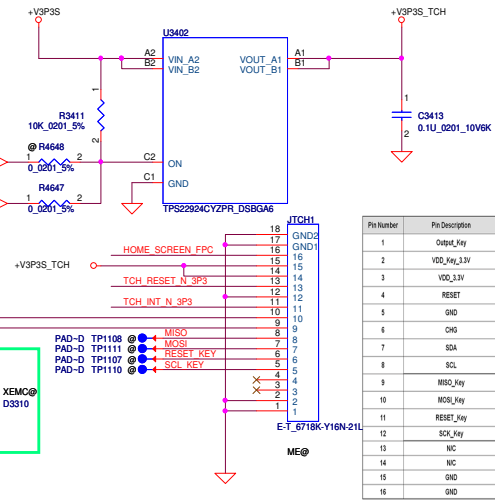


FB4 for SDV 11.6" panel verify

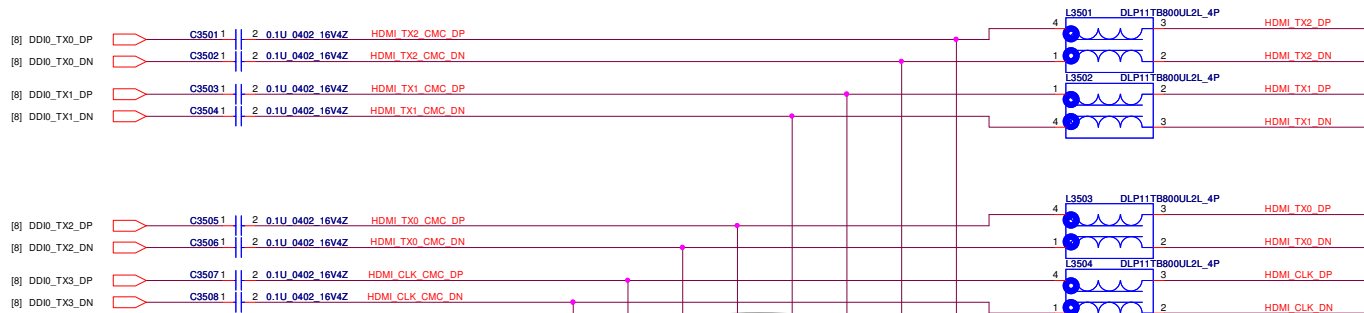
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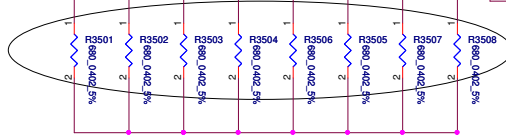
Add to transfer +V3P3S_EDP.0108.



Pin Number	Pin Description
1	Output_Key
2	VDD_Key_3.3V
3	VDD_3.3V
4	RESET
5	GND
6	CHG
7	SSA
8	SCL
9	MISO_Key
10	MOSI_Key
11	RESET_Key
12	SDA_Key
13	NC
14	NC
15	GND
16	GND



Follow REV0.9 Schematics 619->680

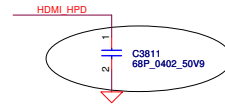


5/13 change PN to SM070002000

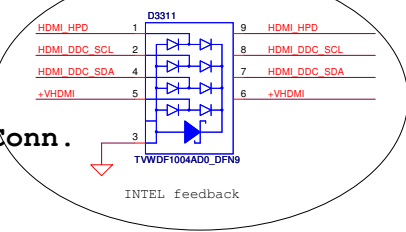
[11.34,99.48] SLP_S00X_N

Q3501
DMG1012T-7_S0T523-3
Vgs = 1v (Max.)

10/19 add de-bounce cap on HDMI_HPD (intel review)

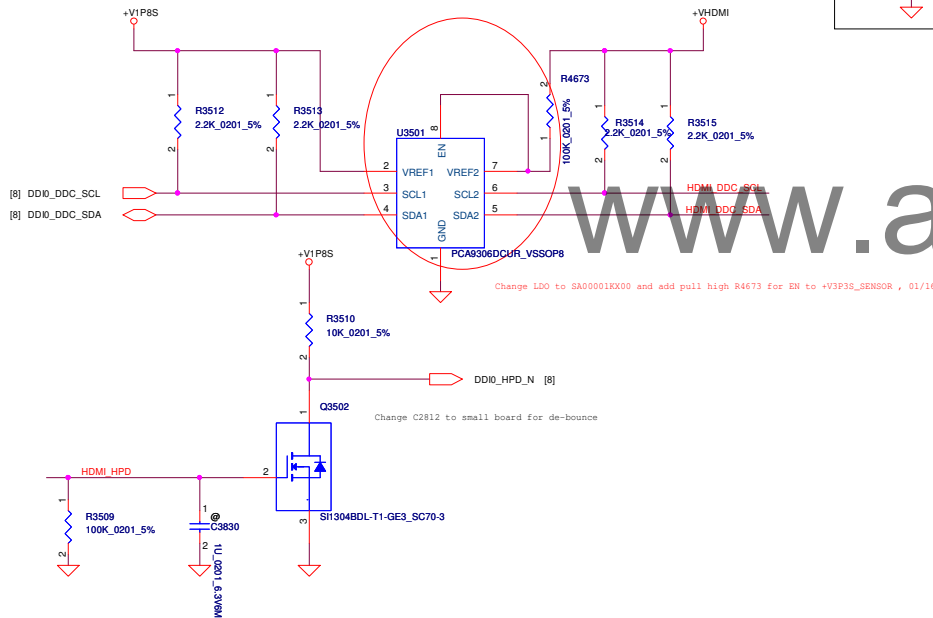


HDMI Conn.



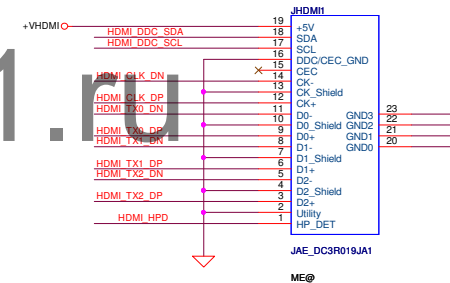
INTEL feedback

Net name change.0111.



Change LDO to SA00001KX00 and add pull high R4673 for EN to +V3P3_SENSOR , 01/16

Change C2812 to small board for de-bounce

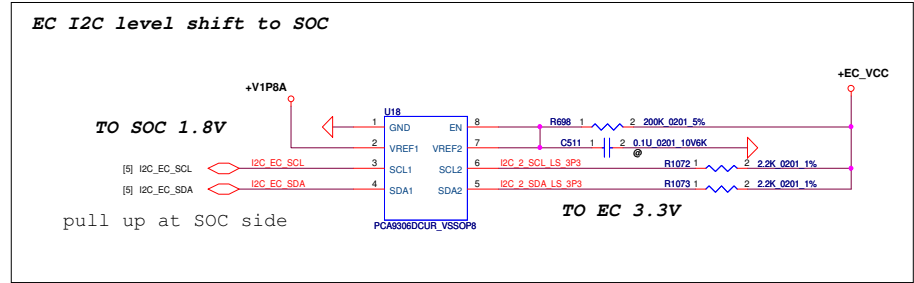
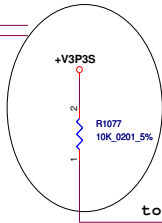
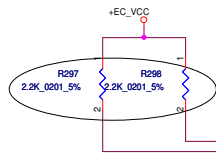


JAE_DC3R019JA1
ME@

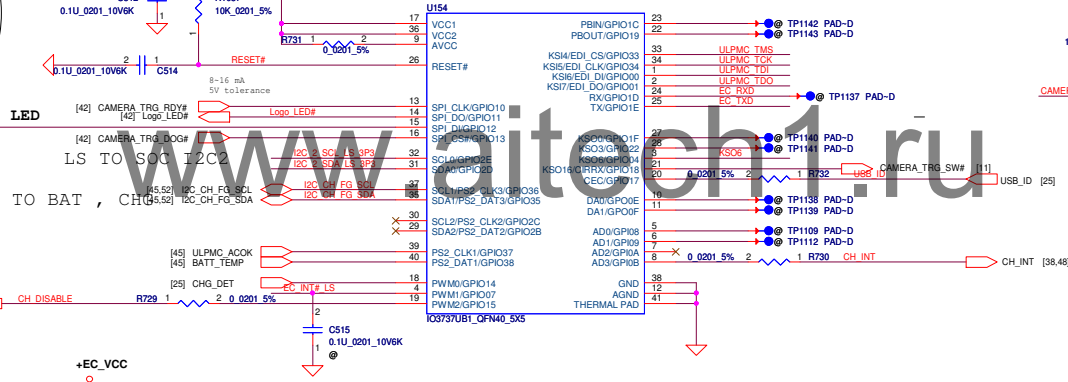
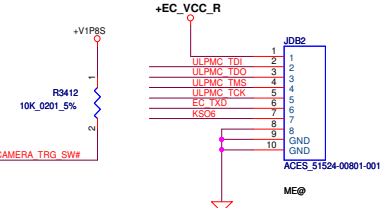
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						Size		Document Number	
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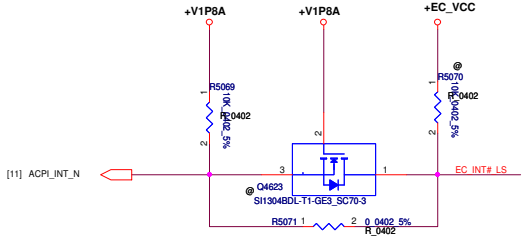
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EC_DEBUG CONN
for update firmware

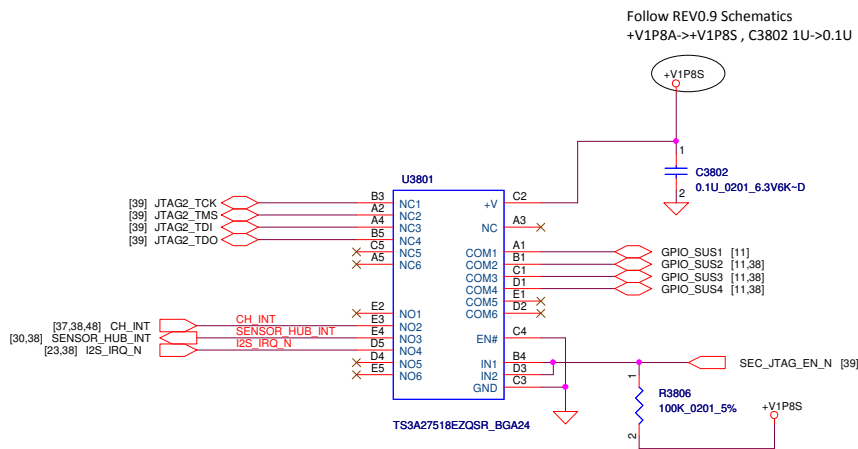


for Charger control

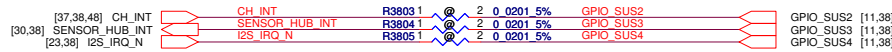


GPI007/GPIO18 setting to OD

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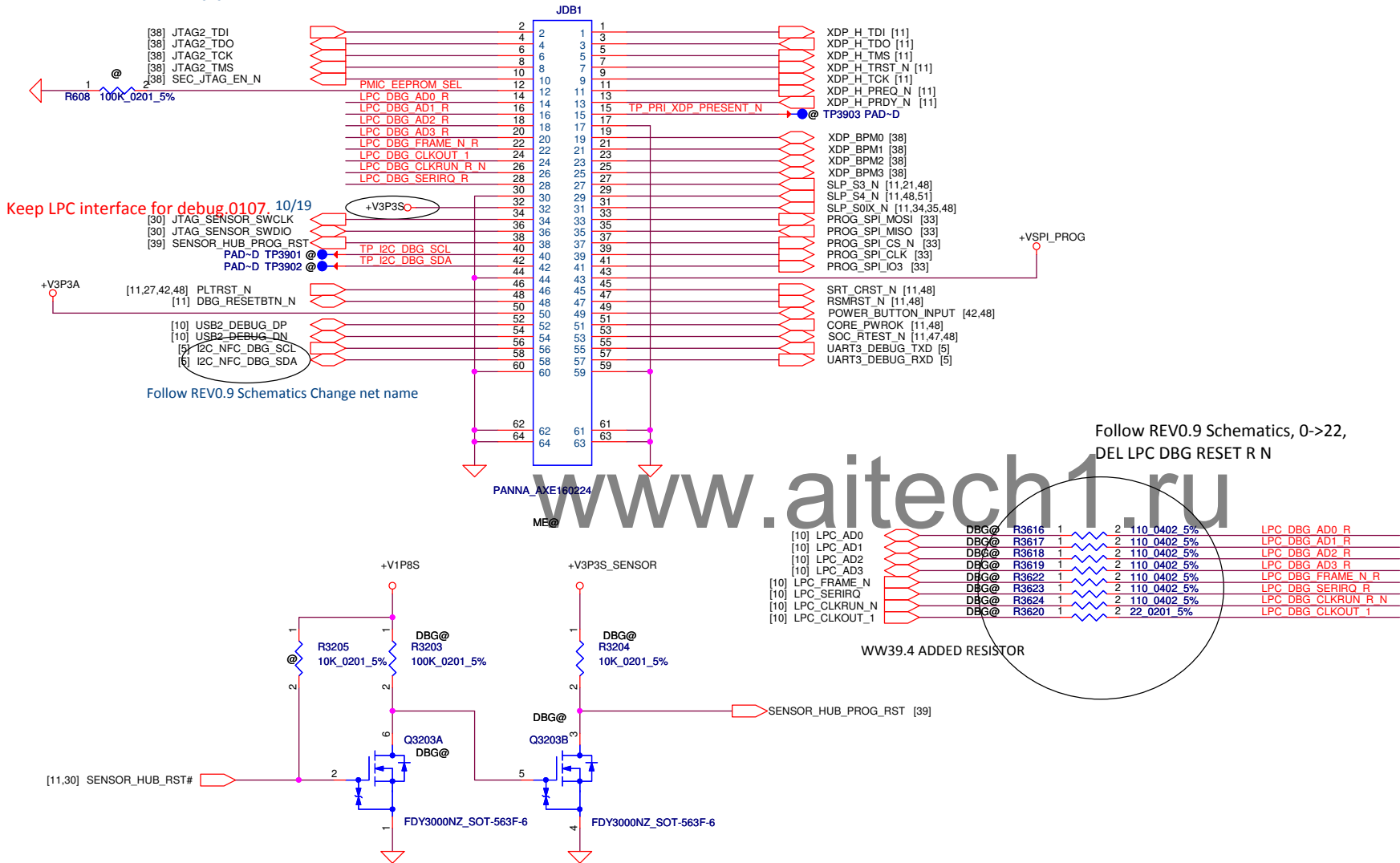
Follow REV0.9 Schematics
change net name



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WW39.4 : CHANGED THE CONNECTIONS ON PIN 10 AND 12

Follow REV1.2

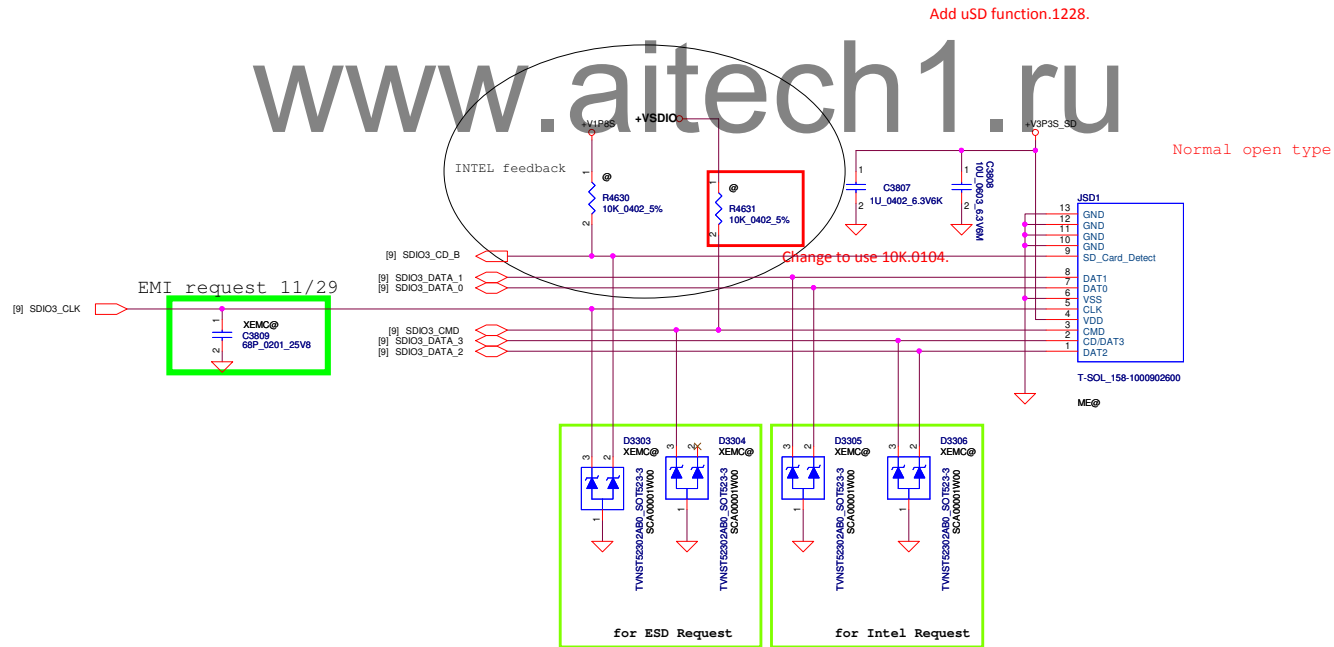
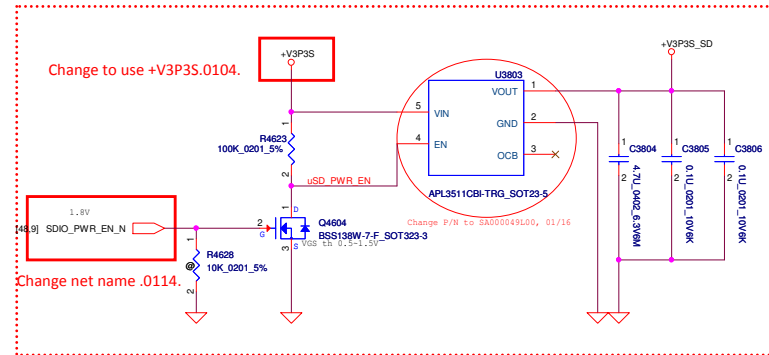
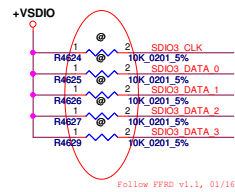


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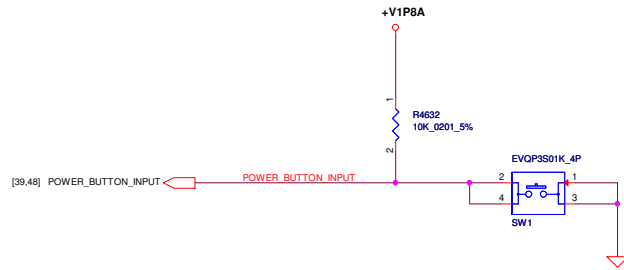
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Micro SD

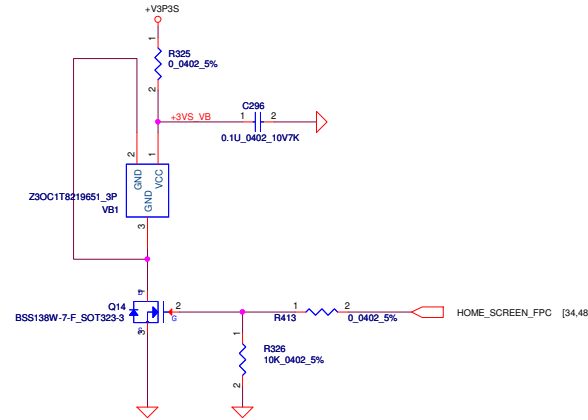


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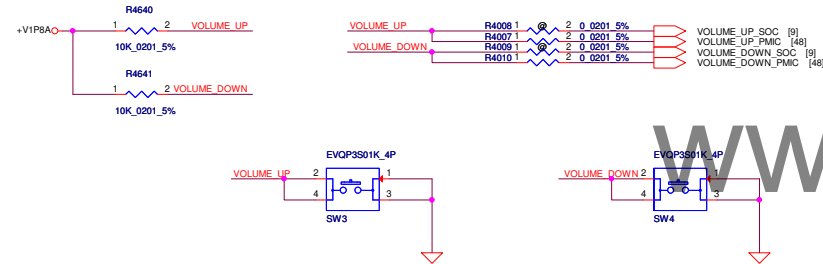
Power SW



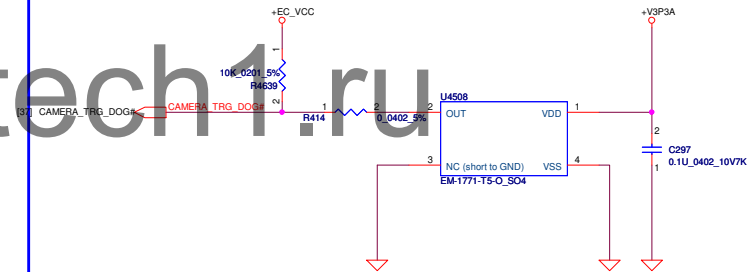
VIBRATOR



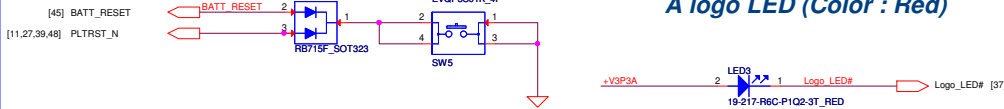
Volume Up/Down



CAMERA LID SENSOR

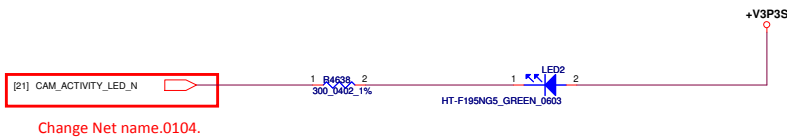


Battery Reset



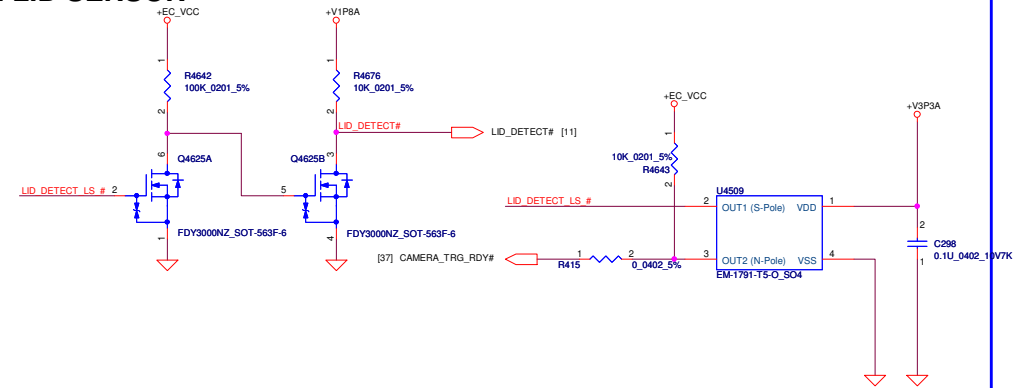
A logo LED (Color : Red)

Camra ON LED

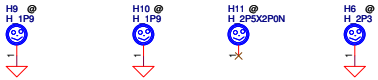
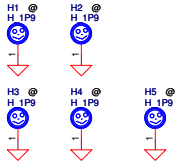
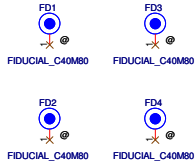
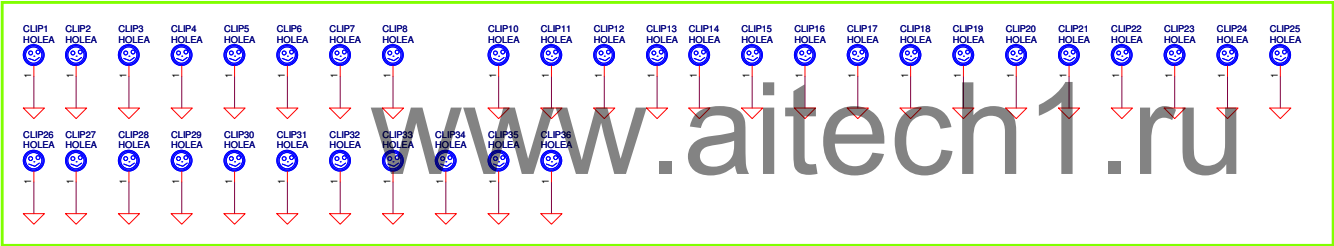


Change Net name.0104.

COVER LID SENSOR

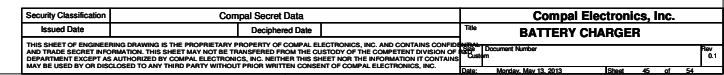


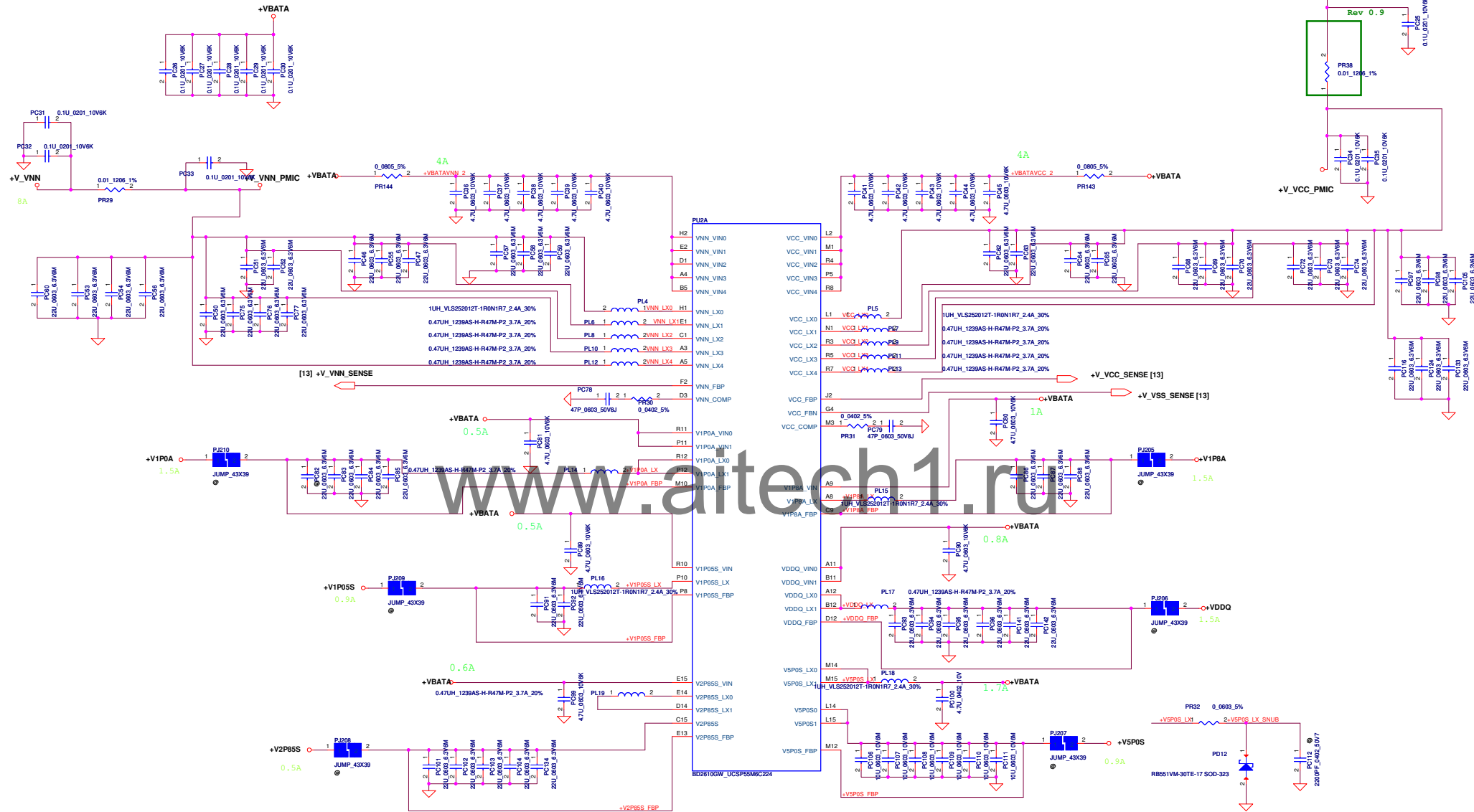
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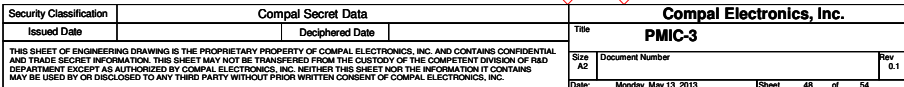
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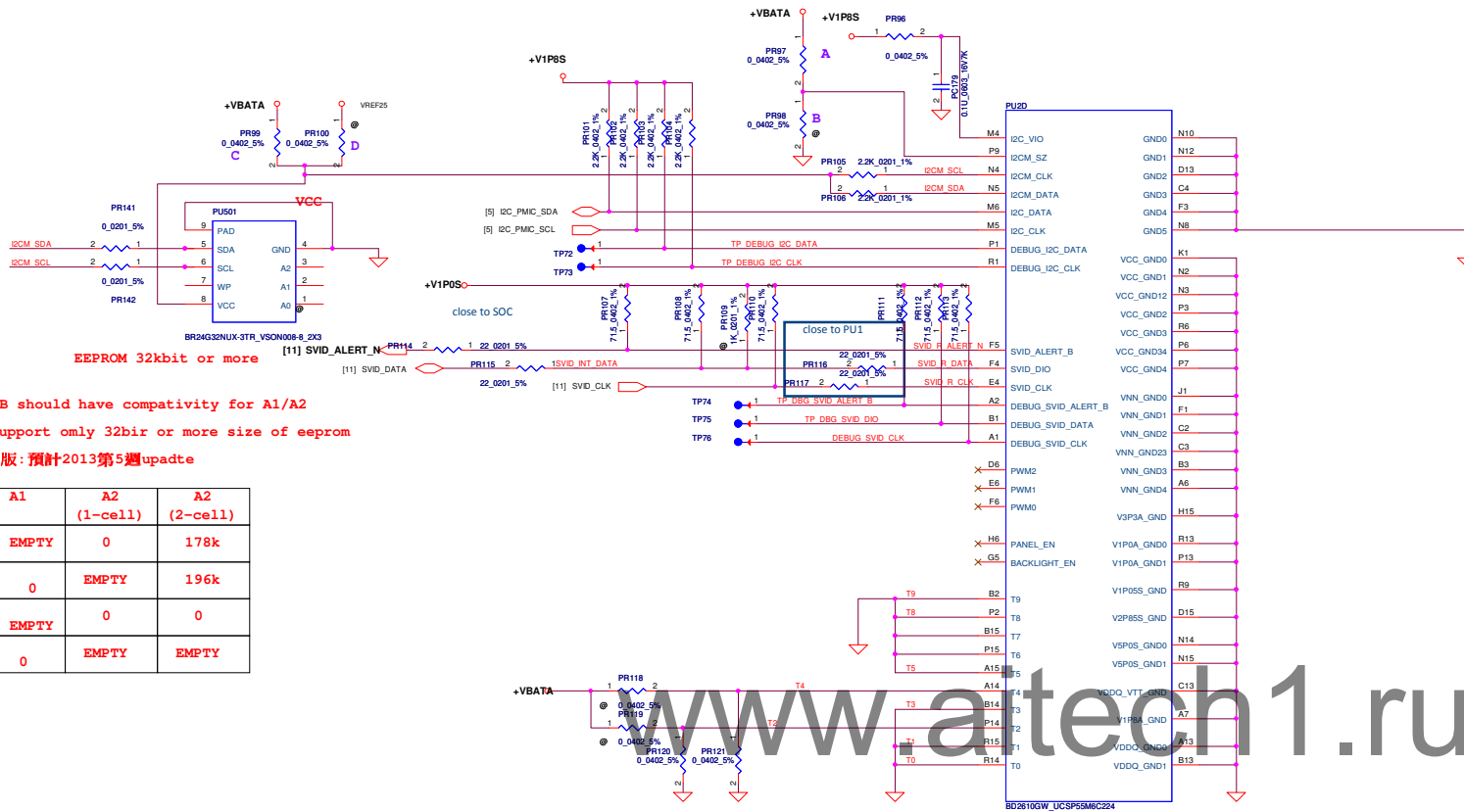
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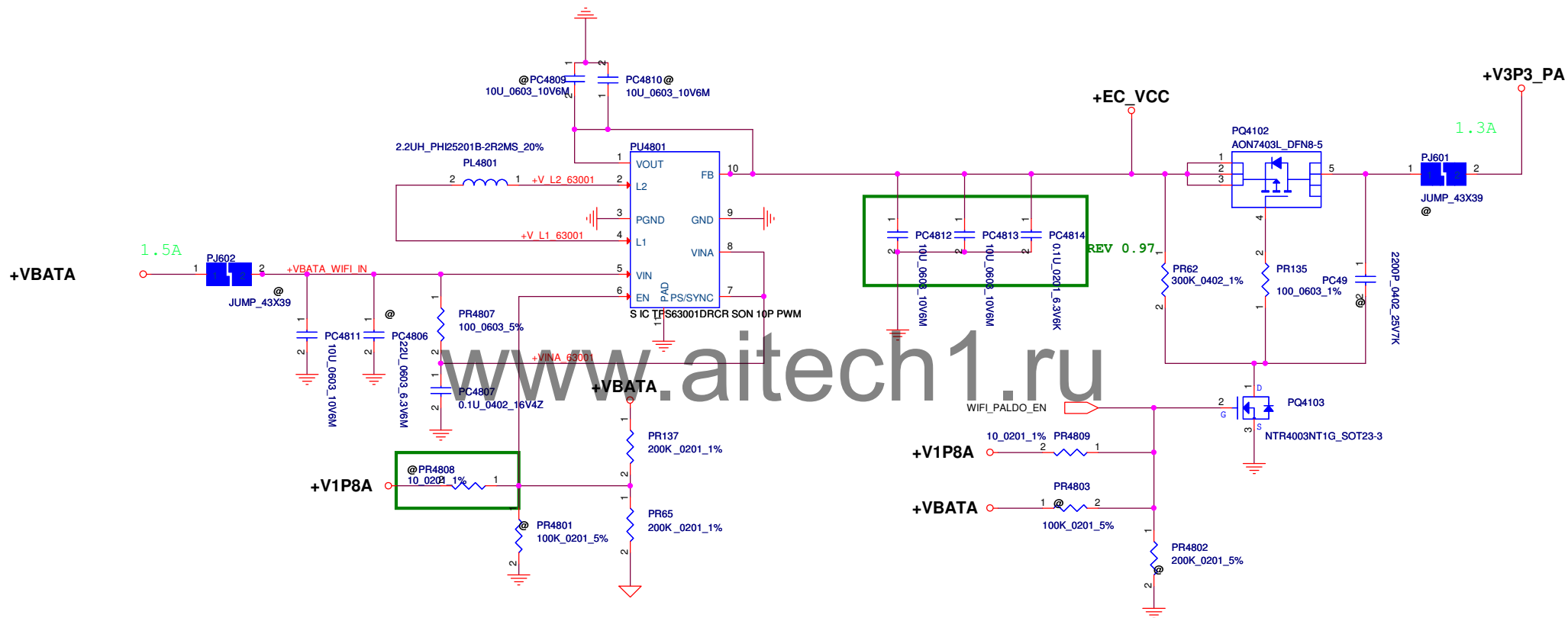




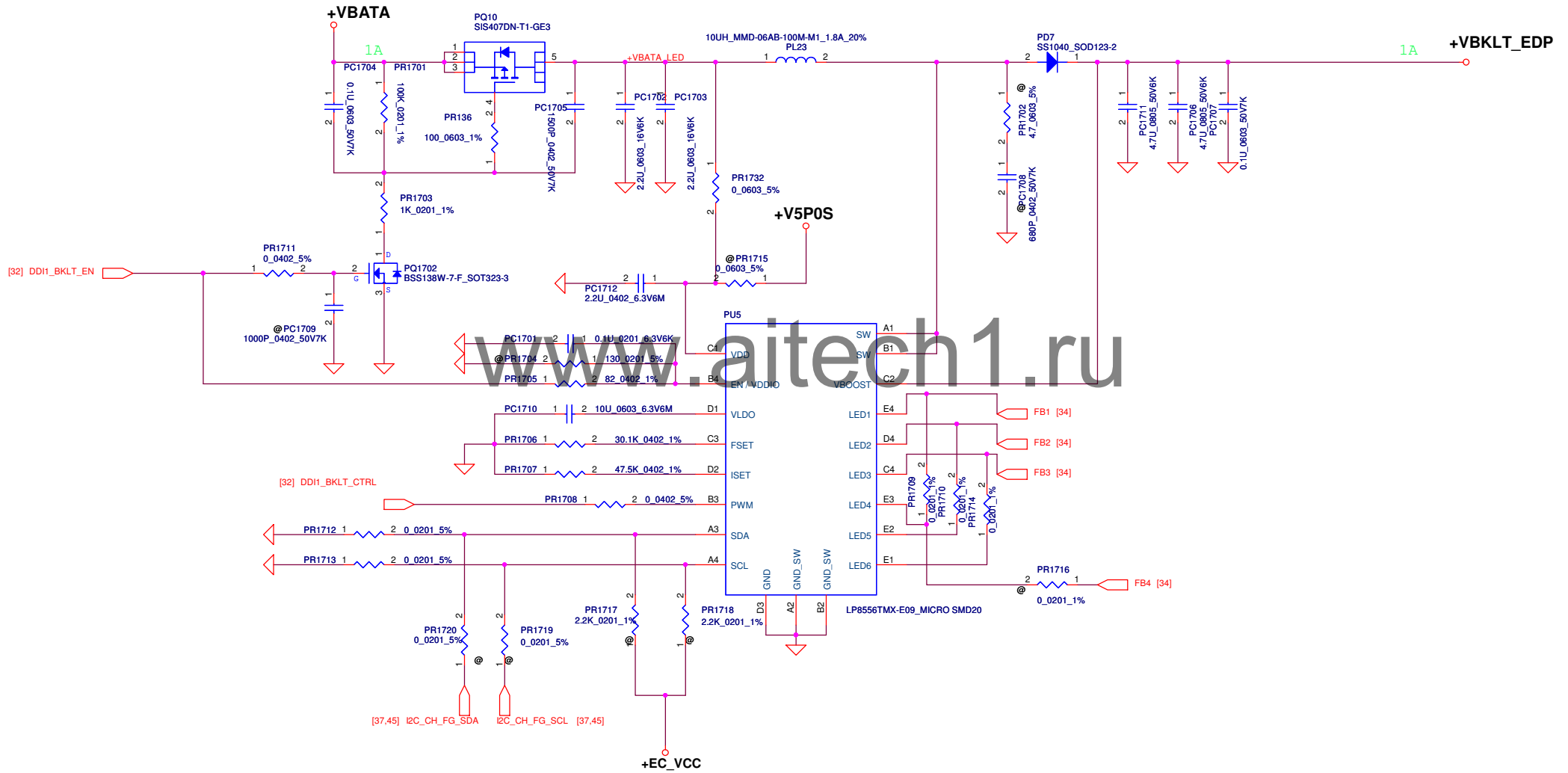
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